AEWIN Advanced Embedded & Network Solutions

User Manual

MB-8390

Mini-ITX support AMD® R-series APU, AMD® A75 chipset, DDR3 up to 16GB, 2 x Intel® Giga LAN, Onboard 3 x HDMI, 1 x DP port, 2 x SATA, 8 x USB, 2 x COM, GPIO, PCI-Express X16 & X1 slots, Cfast socket, Mini-PCIe socket, optional 8 x intrusion detection / TPM 1.2 / Dual BIOS, DC 8V ~ 32V inputs

Ver.	Release Date	Update
1.0	2013.10.21	Release

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For technical supports, please send your inquiry to sales@aewin.com.tw

Packing list

Before use this product, please make sure that the following materials have been shipped.

- 1 x MB-8390 motherboard
- 1 x SATA cable, L/ 200mm (P/N: 46L-SATA11-00)
- 1 x 12V/5V SATA power cable , L/ 150mm (P/N: 46L-IPOW41-00)
- 1 x CD Utility

46L-SATA11-00	46L-IPOW41-00

Model Name	Description
MB-8390A	AMD® R-series APU, A75 chipset, DDR3 up to 8GB, 2 x Giga LAN, 3 x HDMI, 1 x DP port, 2 x SATA, 8 x USB, 2 x COM, CFast socket, Mini-PCIe socket, DC 8V ~ 32V inputs, PCIe X16 slot
MB-8390B	AMD® R-series APU, A75 chipset, DDR3 up to 8GB, 2 x Giga LAN, 3 x HDMI, 1 x DP port, 2 x SATA, 8 x USB, 2 x COM, CFast socket, Mini-PCIe socket, DC 8V ~ 32V inputs, PCIe X16 & X1 slots

* If any of those items are missing or damaged, please contact with sales representative or distributor.

Optional Accessory

Photo	Model Name	
	P/N:	49L-F00055-00
	CPU cooling Fan for AMD® 722-PGA (FS1r2) socket	
	P/N:	RE-S01
	PCI-express riser card support 1 x PCIe X16 & 1 x PCI slots Note: Work with MB-8390B only	
	P/N:	46L-SATA11-00
	SATA cable, L/ 200mm	
	P/N:	46L-IPOW41-00
	12V/5V SATA power cable , L/ 150mm	
	P/N:	46L-IUSB07-AA
	Dual USB cable, L/ 250mm, with bracket	
	P/N:	46L-IPOW102-00
	P4 4-pin to DC Jack lockable power cable, L/ 200mm	

Safety Information

- To prevent electrical shock hazard, disconnect the power cable from the electrical outlet before relocating the system.
- When adding or removing devices to or from the system, ensure that the power cables for the devices are unplugged before the signal cables are connected. If possible, disconnect all power cables from the existing system before you add a device.
- Before connecting or removing signal cables from the motherboard, ensure that all power cables are unplugged.
- Seek professional assistance before using an adapter or extension cord. These devices could interrupt the grounding circuit.
- Make sure that your power supply is set to the correct voltage in your area.
- If you are not sure about the voltage of the electrical outlet you are using, contact your local power company.
- If the power supply is broken, do not try to fix it by yourself. Contact a qualified service technician or your retailer.

Operation Safety

- Before installing the motherboard and adding devices on it, carefully read all the manuals that came with the package.
- Before using the product, make sure all cables are correctly connected and the power cables are not damaged. If you detect any damage, contact your dealer immediately.
- To avoid short circuits, keep paper clips, screws, and staples away from connectors, slots, sockets and circuitry.
- Avoid dust, humidity, and temperature extremes. Do not place the product in any area where it may become wet.
- Place the product on a stable surface.
- If you encounter technical problems with the product, contact a qualified service technician or your retailer.

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1.1 Introduction

MB-8390 is a Mini-ITX motherboard support AMD® Embedded R-series APU with AMD Radeon™ HD 7000G series Graphics. Integrated graphics include 3 x HDMI + 1 x DP port, Two DDR3 SO-DIMM supports a maximum of 16GB DDR3 1600 of system memory.

On the I/O ports, the MB-8390 provides plenty of connectivity with 2 x Intel® i211AT GbE LAN controller, 2 x RS232, 2 x USB3.0 + 6 x USB2.0, HD Audio, 2 x SATA, CFast socket, 8-bit GPIO, optional onboard 8 x intrusion detection & TPM 1.2 function. The MB-8390 accepts a wide range 8V ~ 32V DC input suitable for a variety of applications in digital signage, POS, kiosks.

Besides standard PCIe X16 and Mini-PCIe socket, AEWIN's Mini-ITX delivers flexible PCIe X1 expansion slot allowing customers to install AEWIN's riser card for an additional 1 ~ 3 PCIe + PCI slots for various application.

AEWIN also have our own firmware team that could provide customize BIOS service, such as security boot function for gaming application……..

About AEWIN Technologies Co., Ltd.

AEWIN offers reliable and solid products which are produced under Management System Standards: ISO9001-2000 Certificate. The certificate keeps us focused on our quality objectives of management and environmental production. Its willingness to customize standard products for meet unique customer needs makes AEWIN different. All ODM projects are welcome. Years of experiences enables AEWIN to fulfill the customer's vision, by delivering products to exact specifications. AEWIN R&D team is proud of its strong engineering background. R&D professionals account for 25% of the AEWIN workforce. We focus on developing new products for both emerging and established markets.

For more information about OEM/ODM, please contact us :
Email: sales@aewin.com.tw TEL: +886-2-8692-6677

1.2 Specification of board

System	
From Factor	Mini-ITX motherboard
CPU	AMD® Embedded R-series APU - FS1r2 PGA
Chipset	AMD® A75 controller Hub
Memory	2 x DDR3 SO-DIMM / 1600 MHz up to 16GB, without ECC support
BIOS	AMI SPI BIOS. (Optional for dual SPI BIOS)
SSD	1 x CFast socket
Watchdog timer	255 levels, 1 ~ 255 sec
Expansion	1 x PCI-Express X16 slot (**Support PCIe X8 signal only**) 1 x PCI-Express X1 slot (**MB-8390B only**) 1 x Full-size Mini-PCIe socket (Support USB, PCIe or SATA signal)
Board Size	170mm x 170mm
Operating Temp.	0°C~60°C (32°F~140°F)
Storage Temp.	.-20°C~80°C (-4°F~176°F)
Operating Hum.	10%~90% (non-condensing)

Display	
Chipset	AMD® A75 controller Hub build in AMD® Radeon HD 7000G series graphic
Display interface	3 x external HDMI
	1 x external DP port

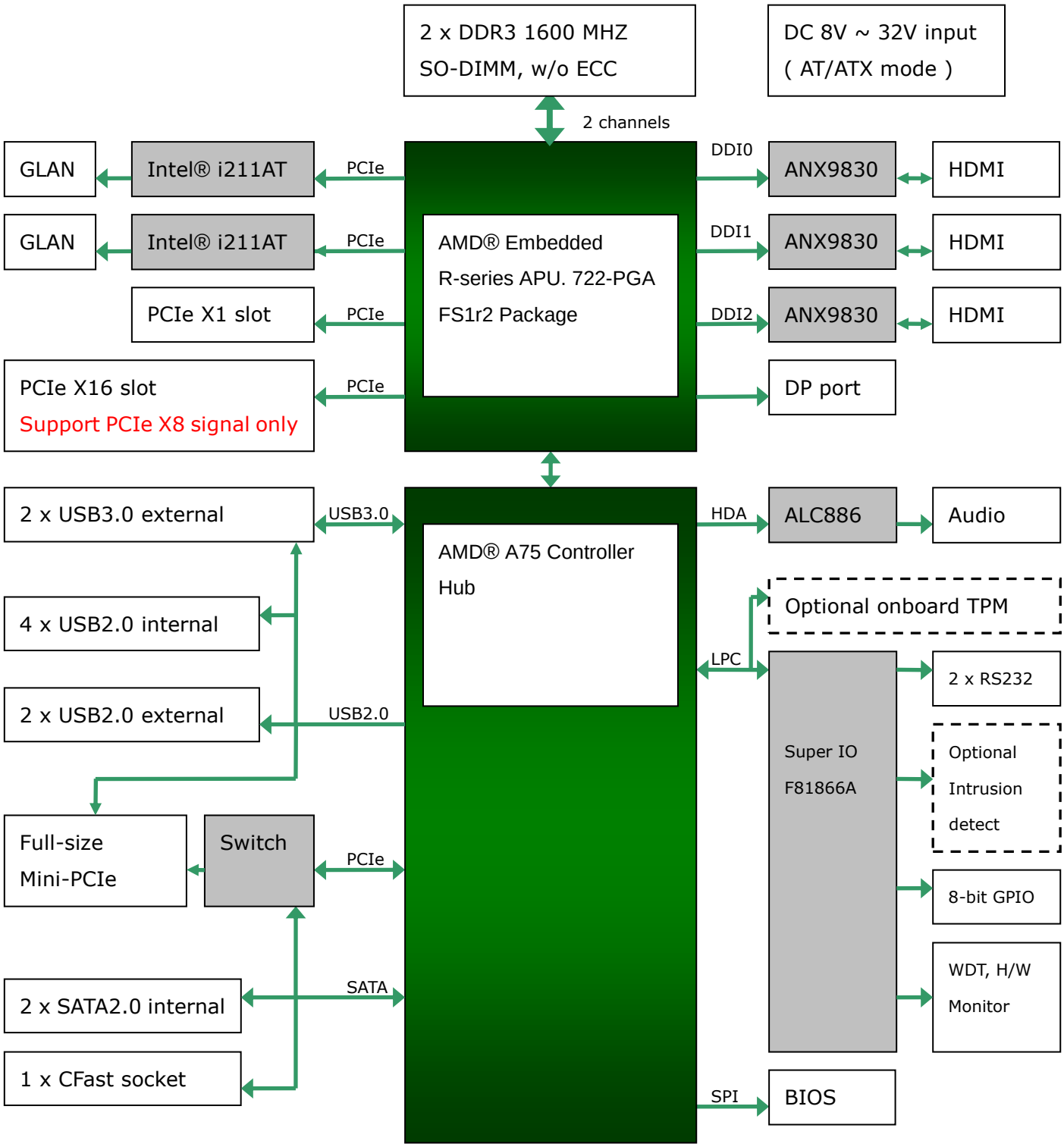
I/O	
Series Port	Internal : 2 x RS232
SATA	2 x SATAII-300MB/s
USB	External : 2 x USB3.0 (compatible with USB 2.0) + 2 x USB2.0 Internal : 4 x USB2.0
Ethernet	External : 2 x Intel I211AT Gigabit Ethernet
Audio	Line-Out, Line-In , Mic-In
Digital I/O	8-bit GPIO interface
LPC	1 x LPC header for Optional TPM module
Others	1 x 3-pin PWM Fan header 1 x Front Panel header for power on/off, reset, HDD/power LED indicator 2 x 4-pin 12V/5V DC out for SATA HDD 1 x 2-pin for Full-size/Half-size Mini-PCIe LED indicator header

	Optional 8 x intrusion detection & onboard TPM 1.2. (OEM version)

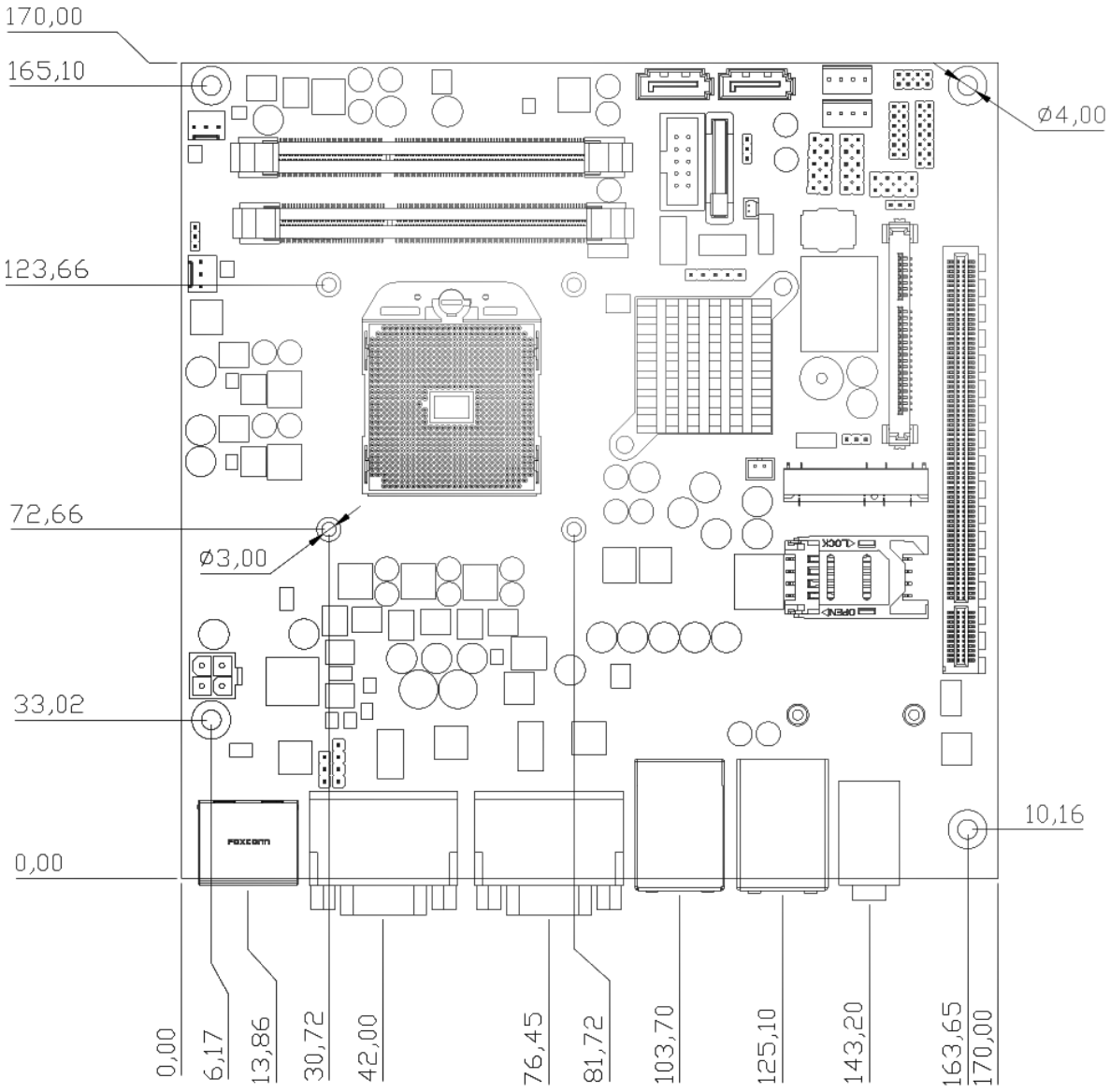
Power	
Power in	DC 8V ~ 32V input (AT/ATX mode jumper selectable)
Power connector	1 x P4 4-pin internal header

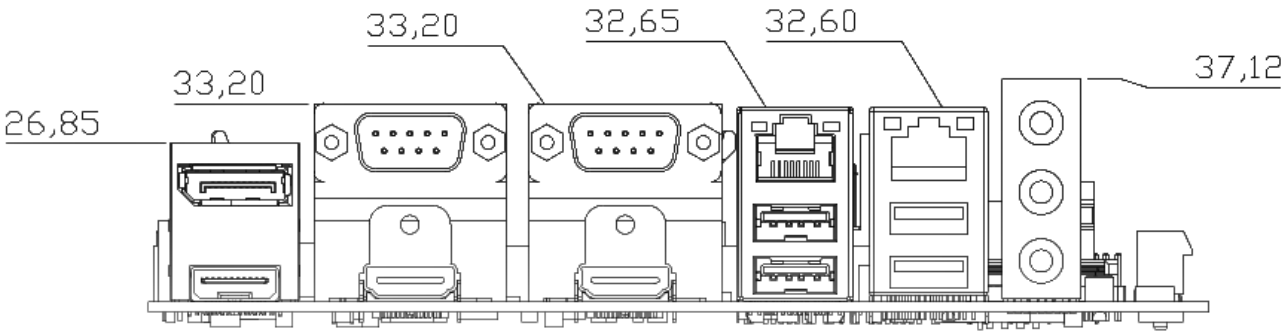
Note : All specifications and photos are subject to change without notice.

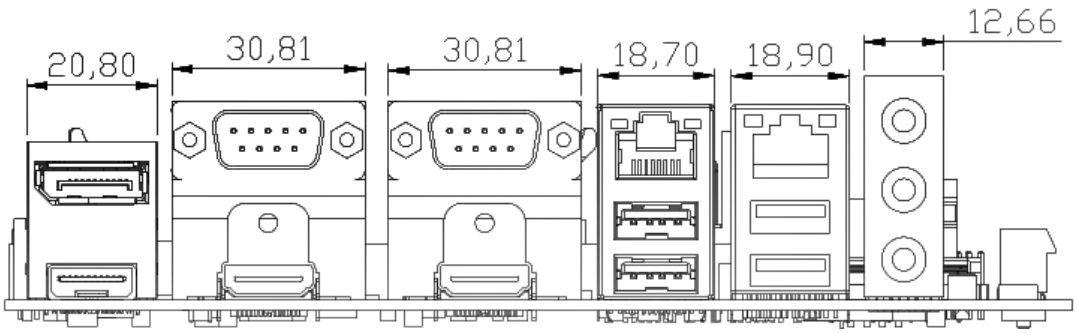
1.3 Block Diagram



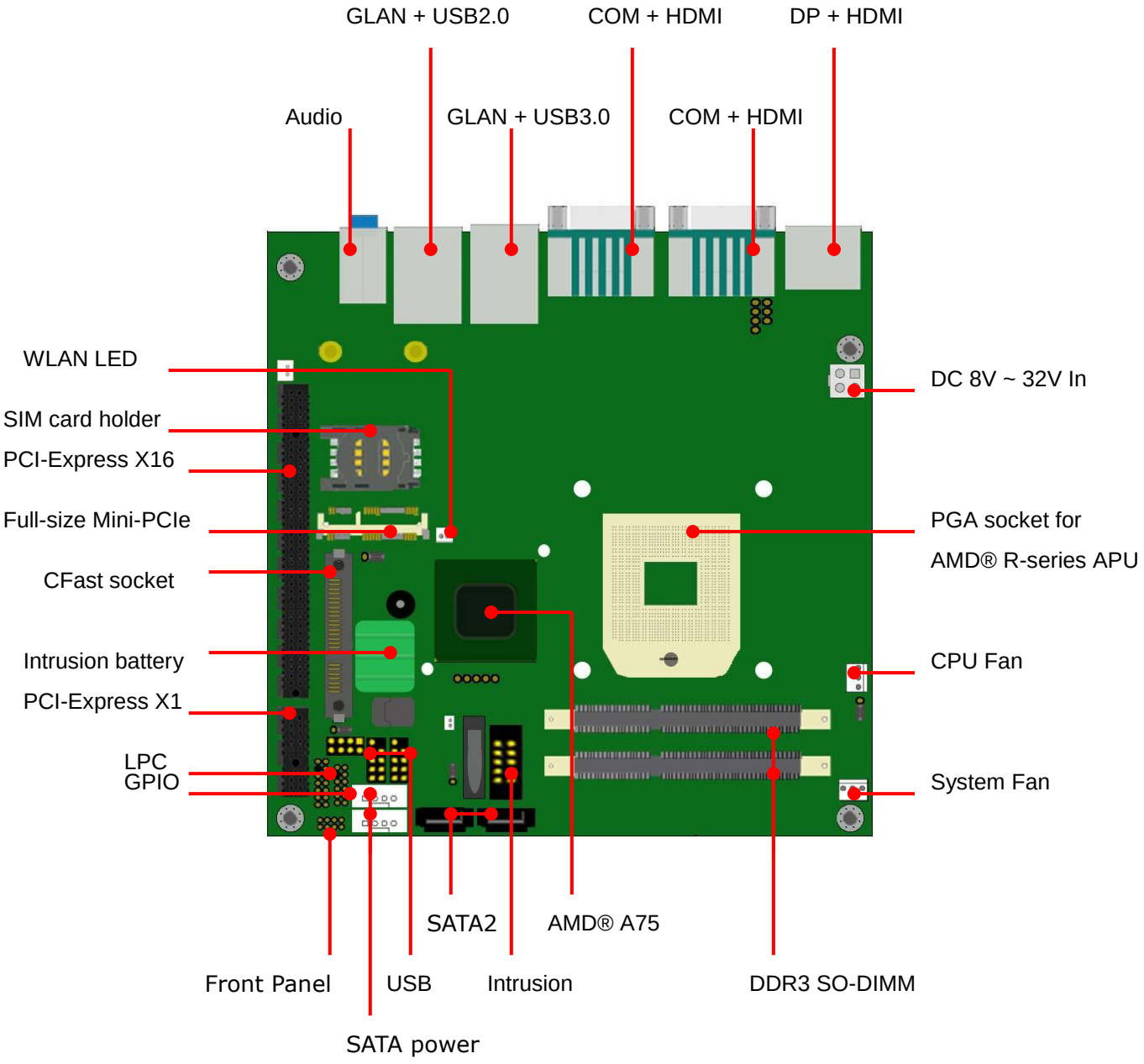
1.4 Board Layout Dimension

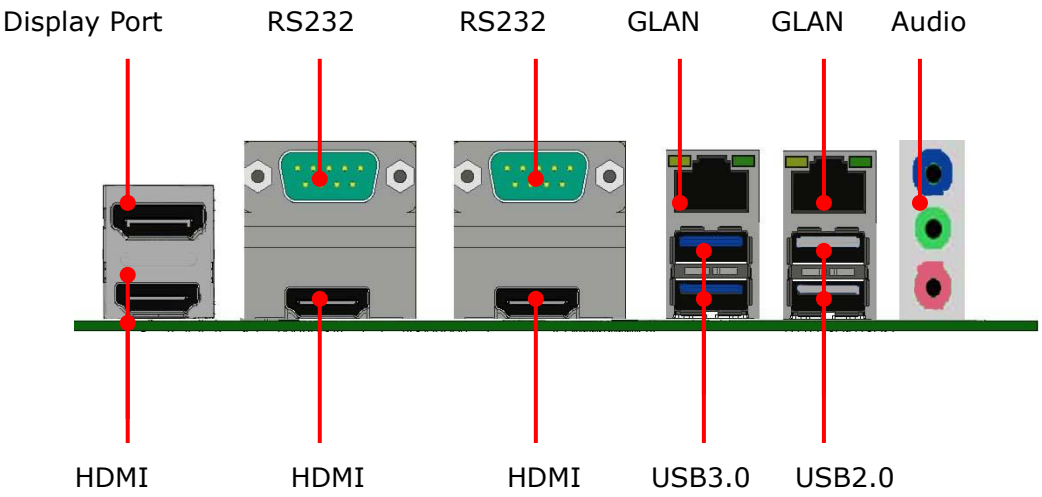



33,20
32,65
32,60
37,12
33,20
26,85

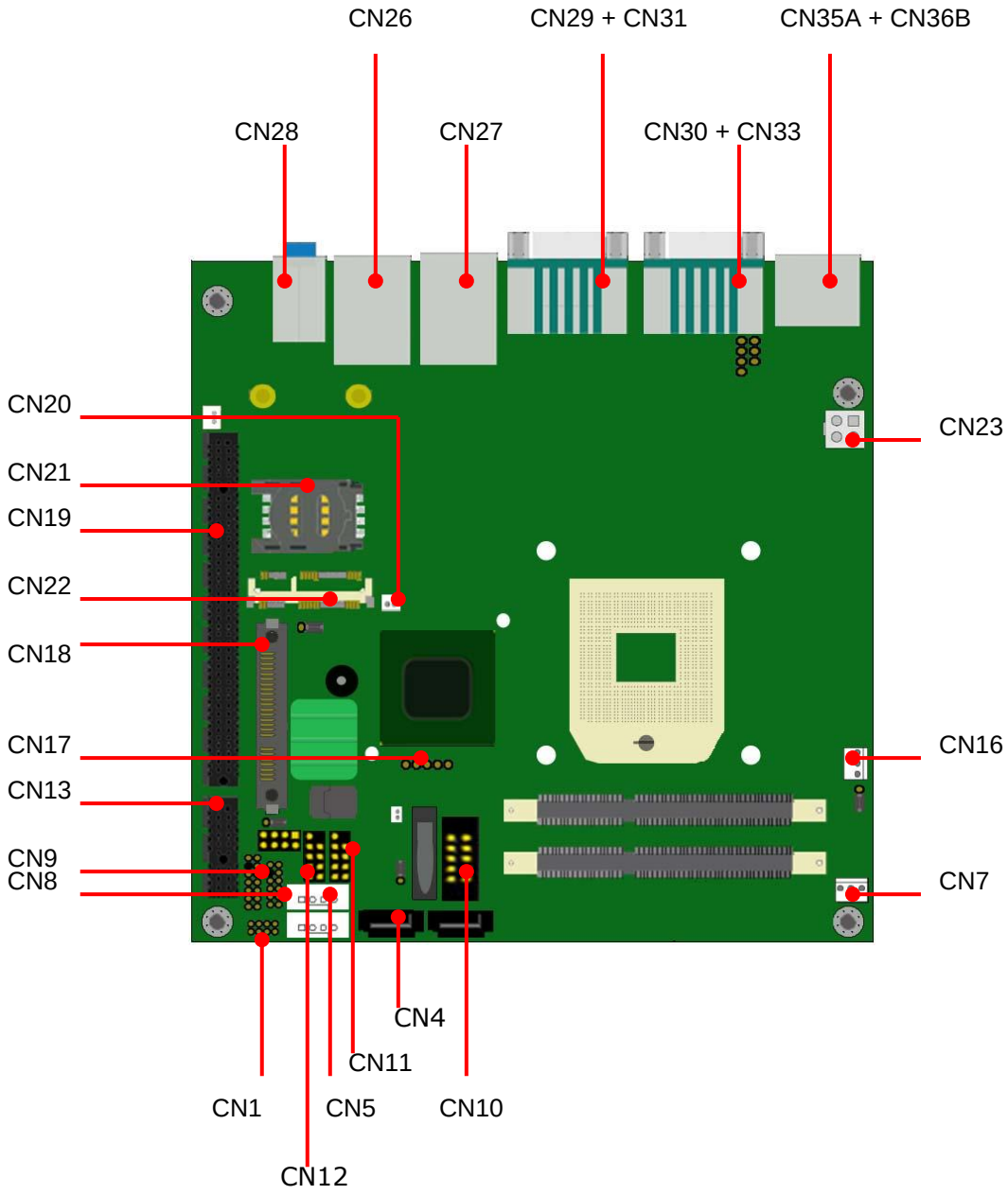

12,66
20,80
30,81
30,81
18,70
18,90

1.5 IO ports


GLAN + USB2.0
COM + HDMI
DP + HDMI
Audio
GLAN + USB3.0
COM + HDMI
WLAN LED
DC 8V ~ 32V In
SIM card holder
PCI-Express X16
Full-size Mini-PCIe
PGA socket for
AMD® R-series APU
CFast socket
Intrusion battery
CPU Fan
PCI-Express X1
LPC
GPIO
System Fan
SATA2
AMD® A75
Front Panel
USB
Intrusion
DDR3 SO-DIMM
SATA power


Display Port
RS232
RS232
GLAN
GLAN
Audio
HDMI
HDMI
HDMI
USB3.0
USB2.0

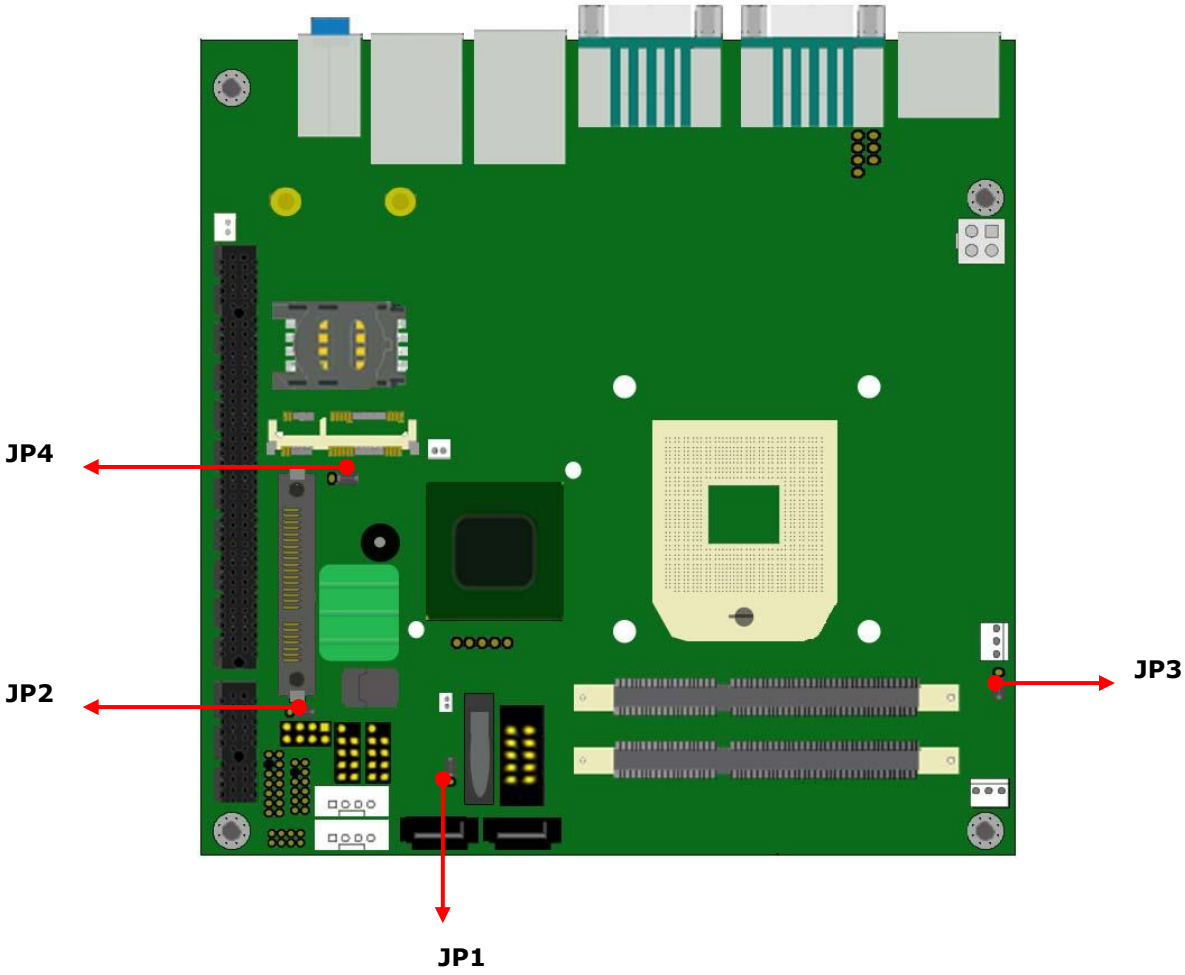
2.1 The location of onboard connectors



Label	Function
CN1	Front panel Pin header
CN2	SATA power connector
CN3	SATA connector
CN4	SATA connector
CN5	SATA power connector
CN6	N/A
CN7	3-pin System Fan connector
CN8	GPIO pin header
CN9	Low Pin Count pin header
CN10	Intrusion detect pin header
CN11	USB2.0 port pin header
CN12	USB2.0 port pin header
CN13	PCI-Express X1 slot
CN14	N/A
CN15	Reserve
CN16	3-pin CPU Fan connector
CN17	Reserve
CN18	CFast socket

Label	Function
CN19	PCI-Express X16 slot
CN20	Mini-PCIe WLAN LED header
CN21	SIM card holder
CN22	Full-size Mini-PCIe socket
CN23	P4 4-pin power connector
CN24	Reserve
CN25	Reserve
CN26	LAN + USB2.0 connector
CN27	LAN + USB3.0 connector
CN28	Audio connector
CN29	COM1
CN30	COM2
CN31	HDMI 2
CN32	N/A
CN33	HDMI 1
CN34	N/A
CN35A	DP port
CN36B	HDMI 0

2.2 The location of onboard jumpers



Label	Function
JP1	CMOS Clear jumper
JP2	CFast card write-protect
JP3	DDR3 voltage selection
JP4	Power AT/ATX mode selection

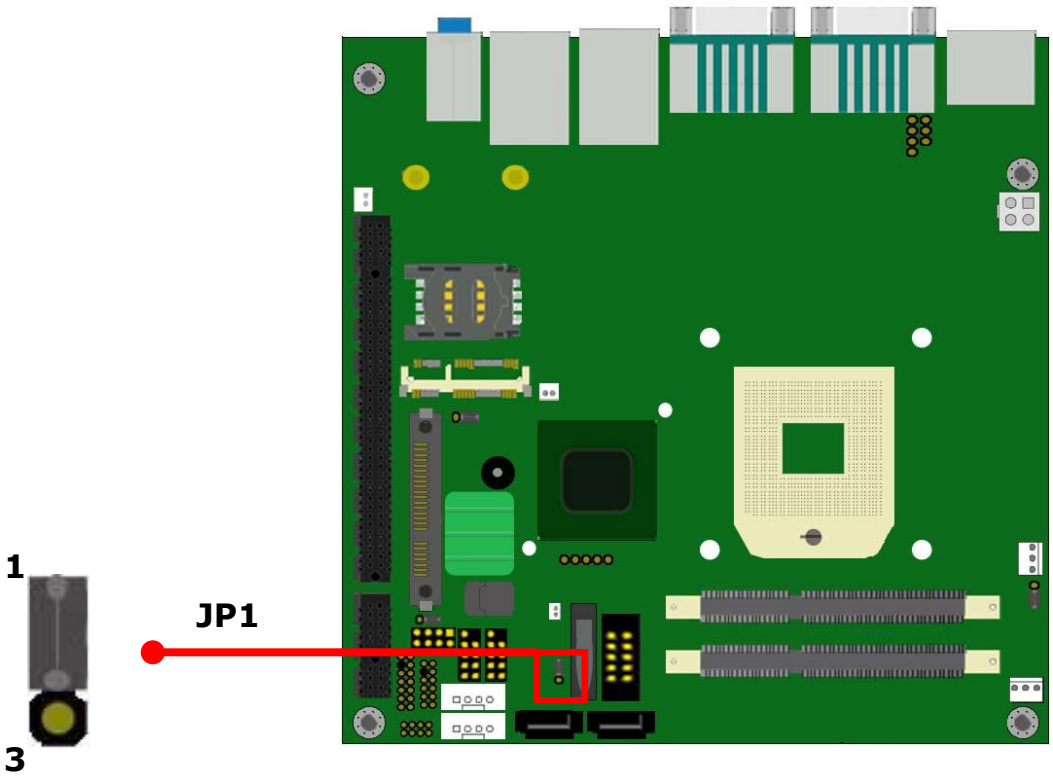
2.3 The function list of onboard jumpers setting

- 2.3.1 : JP1 for for Clear CMOS

If you want to clean the CMOS data, set jumper to 2-3 just for few seconds, Then, Move the jumper back to 1-2 pin

JP1	
Closed Pin	Result
1-2 *	Normal
2-3	Clear CMOS

* Default setting

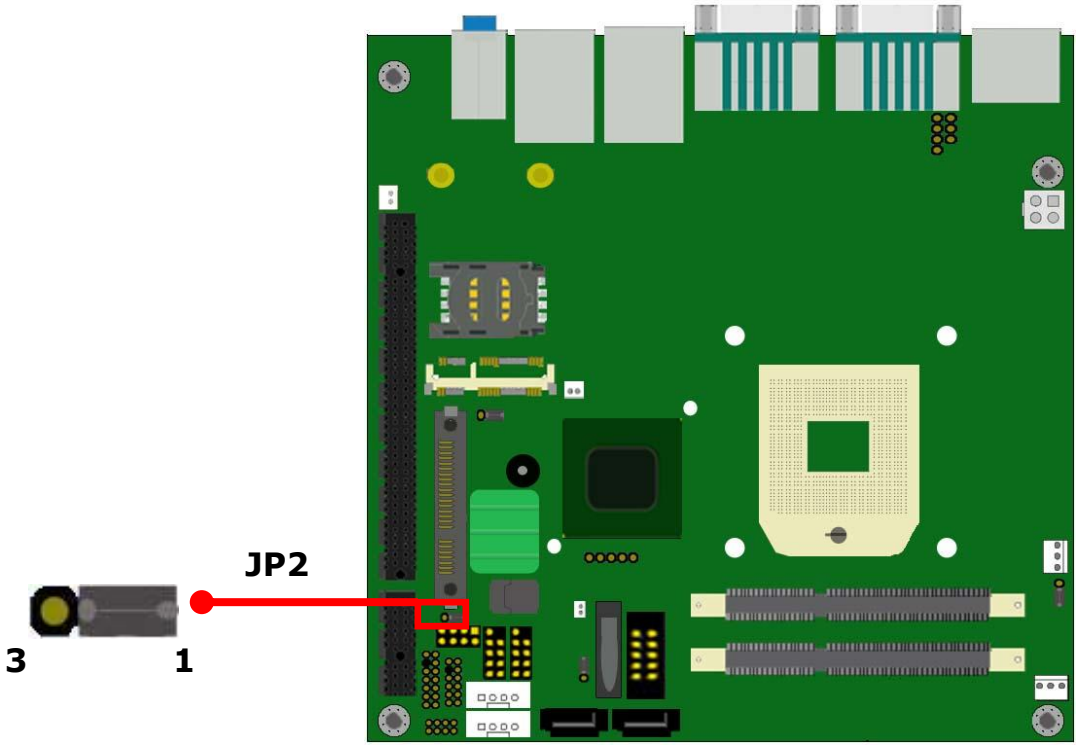


- 2.3.2 : JP2 for CFast write-protect

JP3	
Closed Pin	Result
1-2 *	Can't write the data into CFast card
2-3	Could write data into CFast card

* Default setting

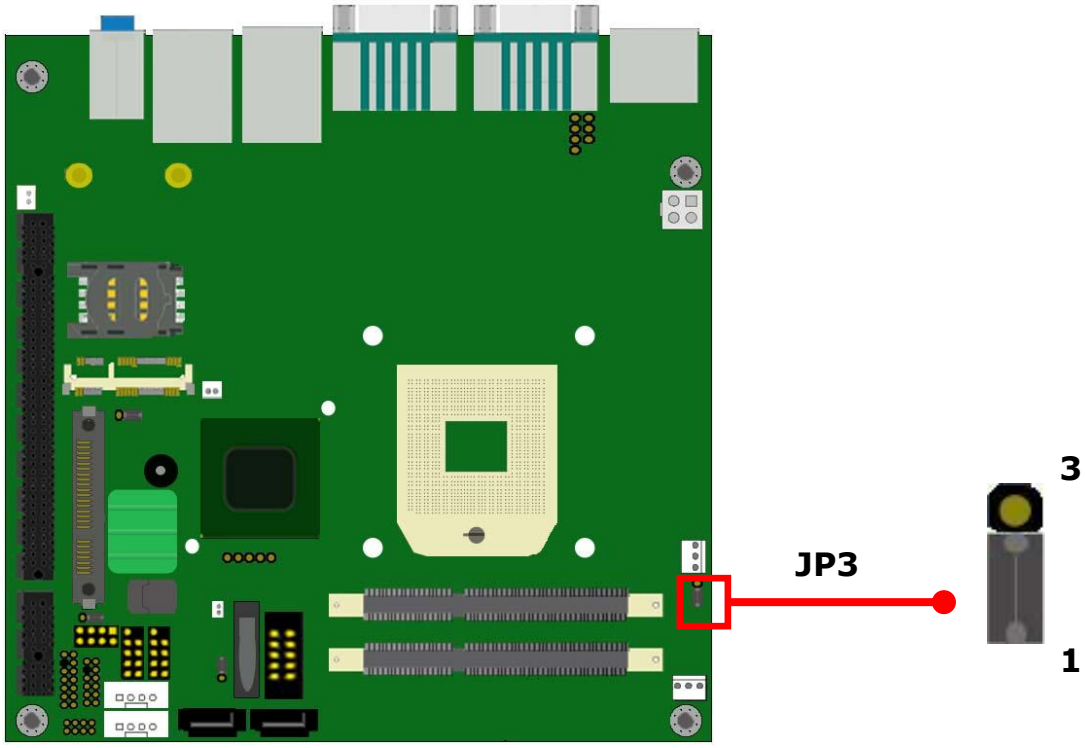
Note: Compatible with a particular brand with a particular model only.
Please check with MB-8390 testing report



-2.3.3 : JP3 DDR3 voltage select

JP4	
Closed Pin	Result
1-2 *	+1.35V
2-3	+1.5V

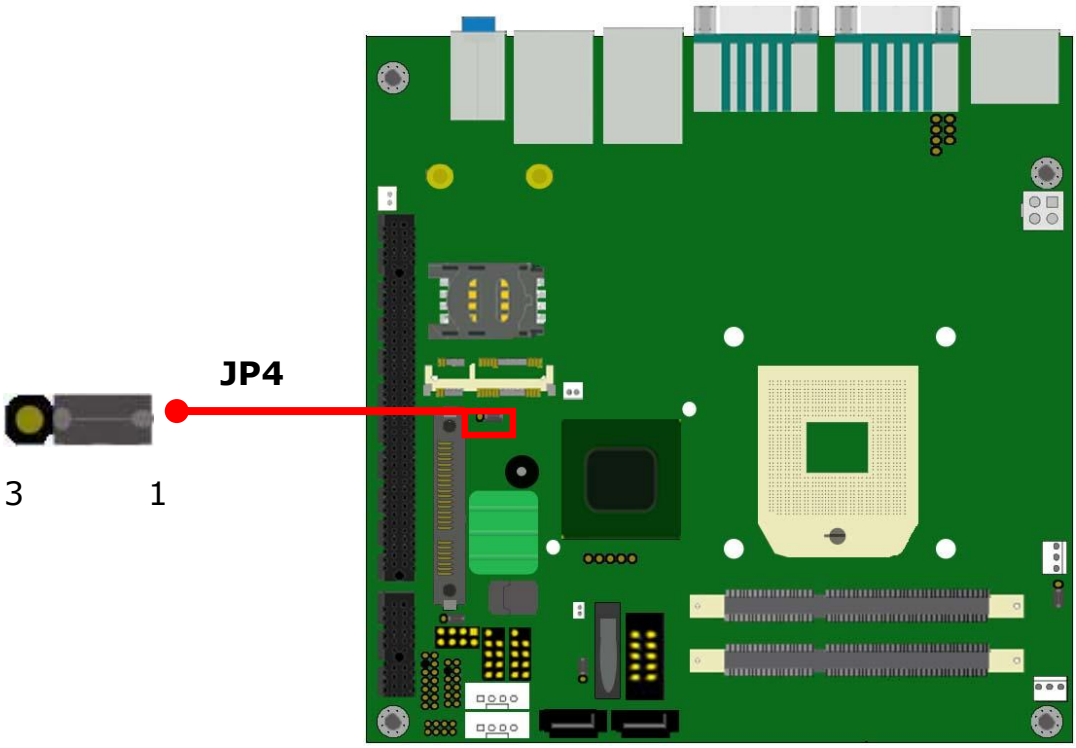
* Default setting



-2.3.4 : JP4 for AT/ATX power mode

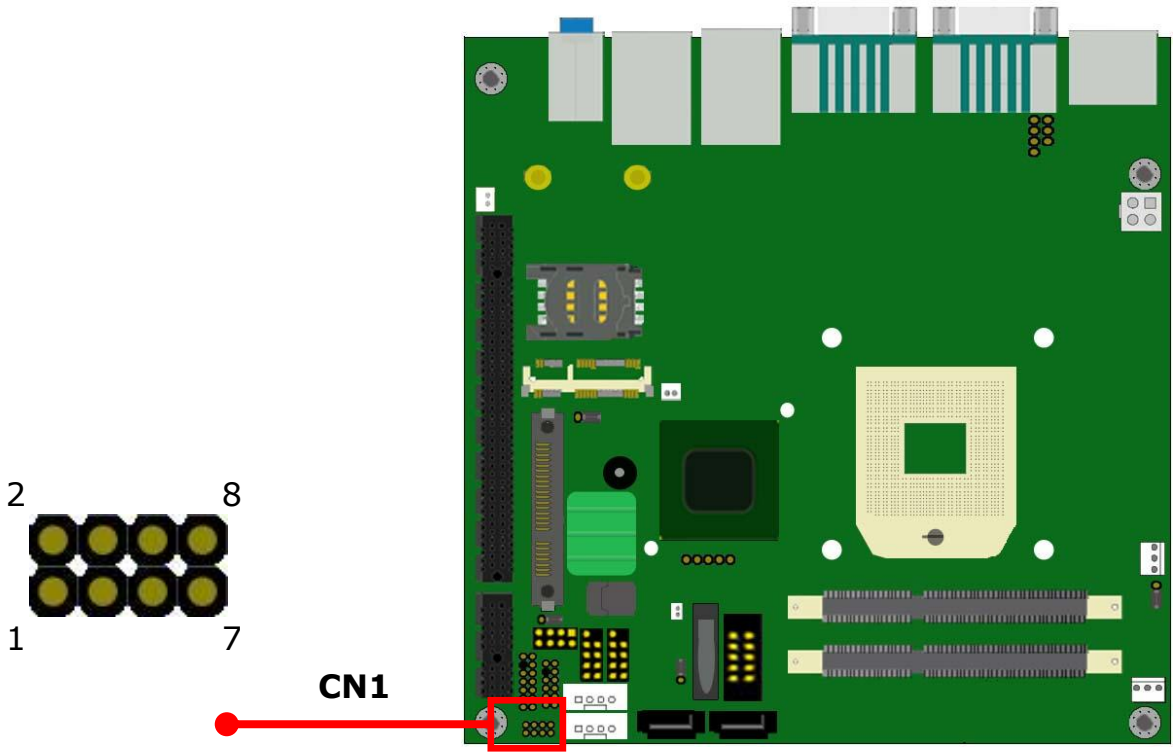
JP5	
Closed Pin	Result
1-2	AT mode
2-3 *	ATX mode

* Default setting



-2.4.1 : CN1 for front Panel pin header

CN16 : 2 x 4 header , pitch 2.00 mm			
Pin	**Signal**	**Pin**	**Signal**
1	Power_LED+	2	GND
3	HDD_LED+	4	HDD_LED-
5	GND	6	Power on/off
7	RESET	8	GND



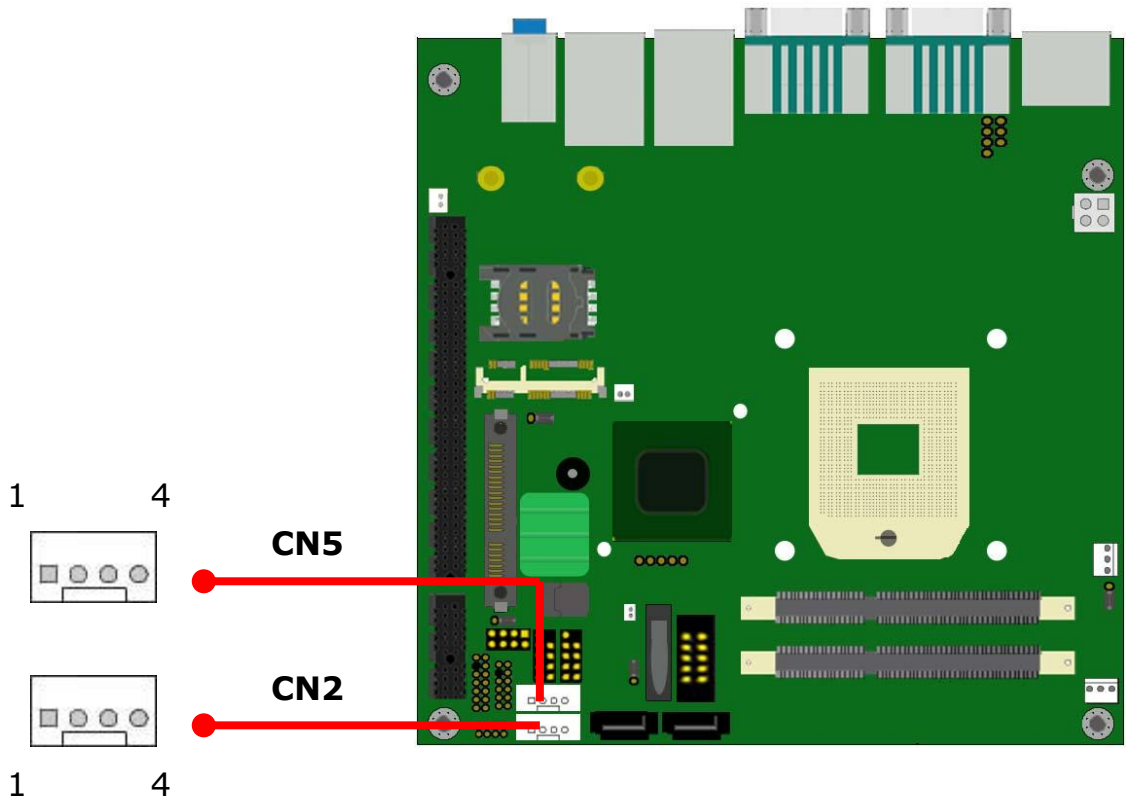
-2.4.2 : CN2 & CN5 for 4-pin HDD power

CN2 : 4-pin wafer for SATA power connector			
Pin	**Signal**	**Pin**	**Signal**
1	+12V	2	GND
3	GND	4	+5V

Note: Maximum output current 12V/1A, 5V/1A

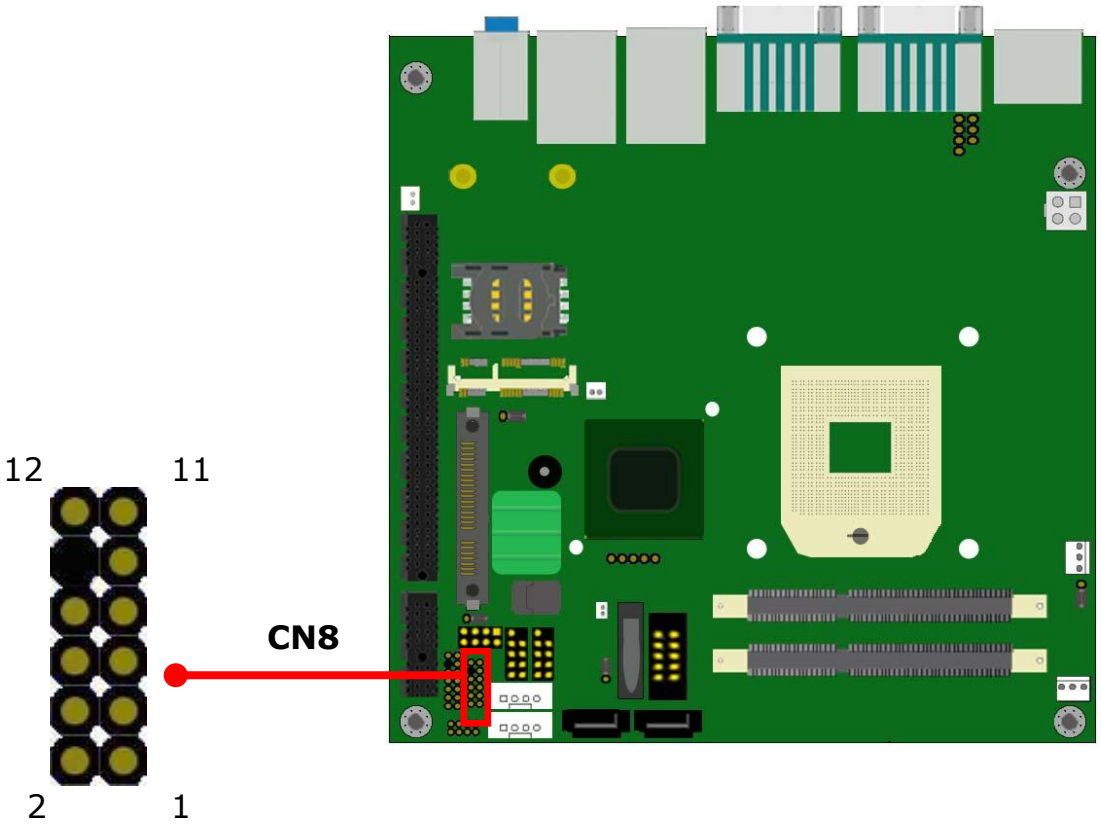
CN5 : 4-pin wafer for SATA power connector			
Pin	**Signal**	**Pin**	**Signal**
1	+12V	2	GND
3	GND	4	+5V

Note: Maximum output current 12V/1A, 5V/1A



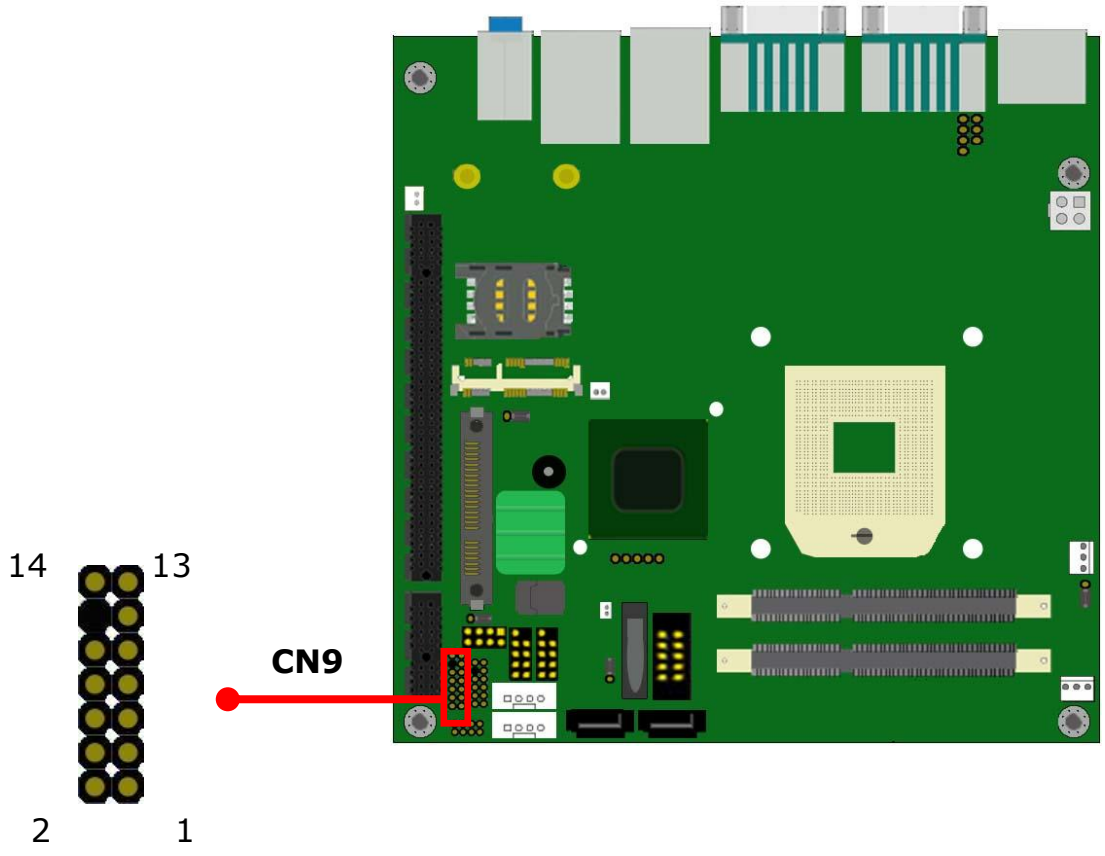
-2.4.3 : CN8 for 8-bit GPIO

CN4 : 2 x 6 header , pitch 2.0 mm			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V	2	GPIO0
3	GPIO1	4	GPIO2
5	GPIO3	6	GPIO4
7	GPIO5	8	GPIO6
9	GPIO7	10	Key
11	+5V	12	GND



-2.4.4 : CN9 for Low Pin Count pin-header

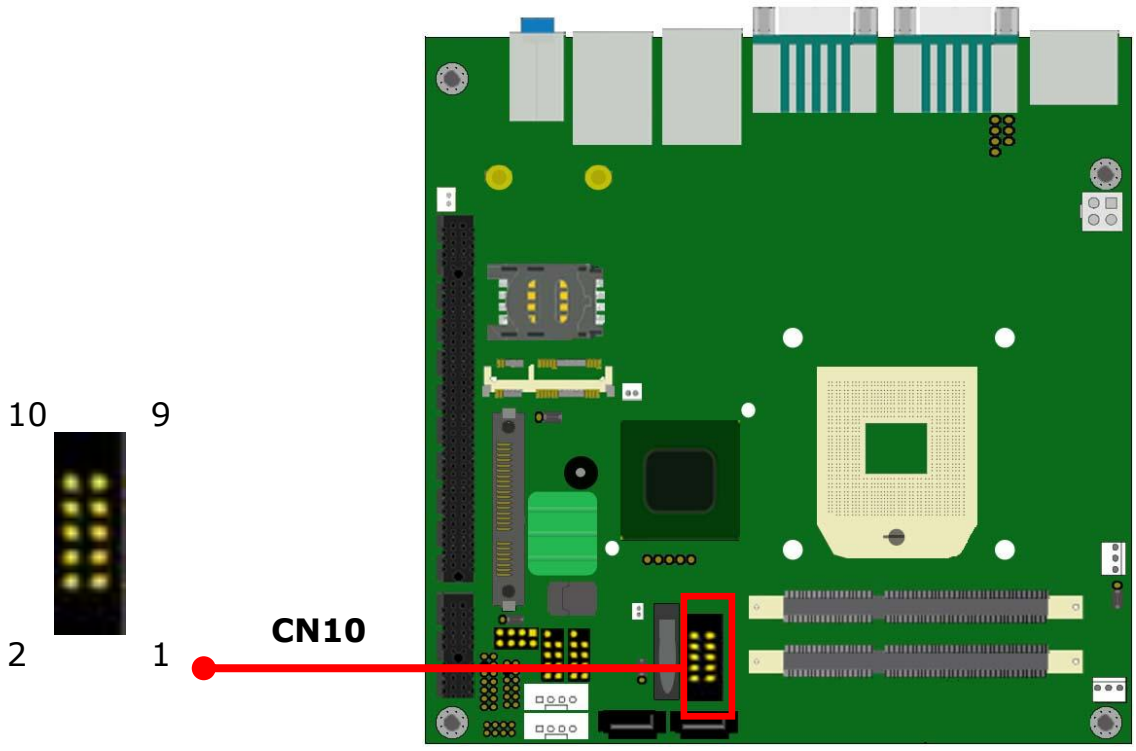
CN9 : 2 x 7 header , pitch 2.0 mm			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V	2	LAD0
3	LAD1	4	LAD2
5	LAD3	6	LFRAME
7	Reset	8	+5V
9	LCLK	10	LPME
11	GND		Key
13	SERIRQ	14	LDRQ



-2.4.5 : CN10 for Intrusion Detection

CN19 : 2 x 5 header, pitch 2.54 mm			
Pin	**Signal**	**Pin**	**Signal**
1	DOOR0	2	DOOR1
3	DOOR2	4	DOOR3
5	DOOR4	6	DOOR5
7	DOOR6	8	DOOR7
9	GND	10	GND

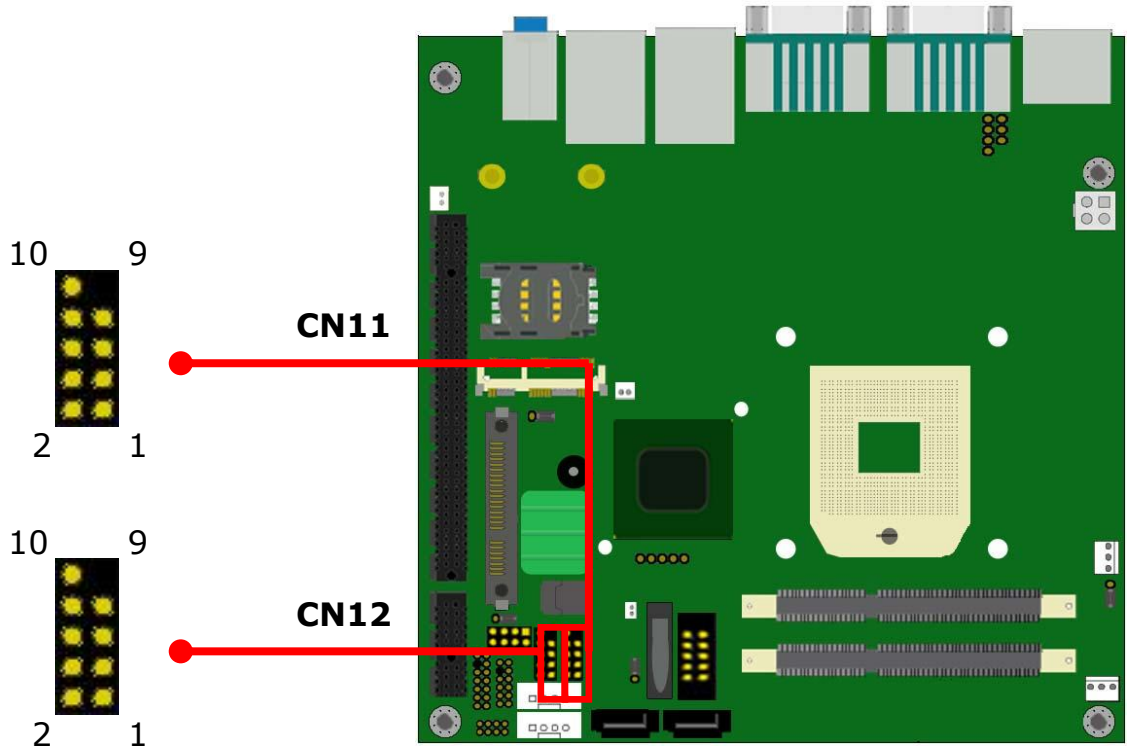
Note: This function for OEM model only



-2.4.6 : CN11 for USB2.0 port 2/3 & CN12 for USB2.0 port 4/5

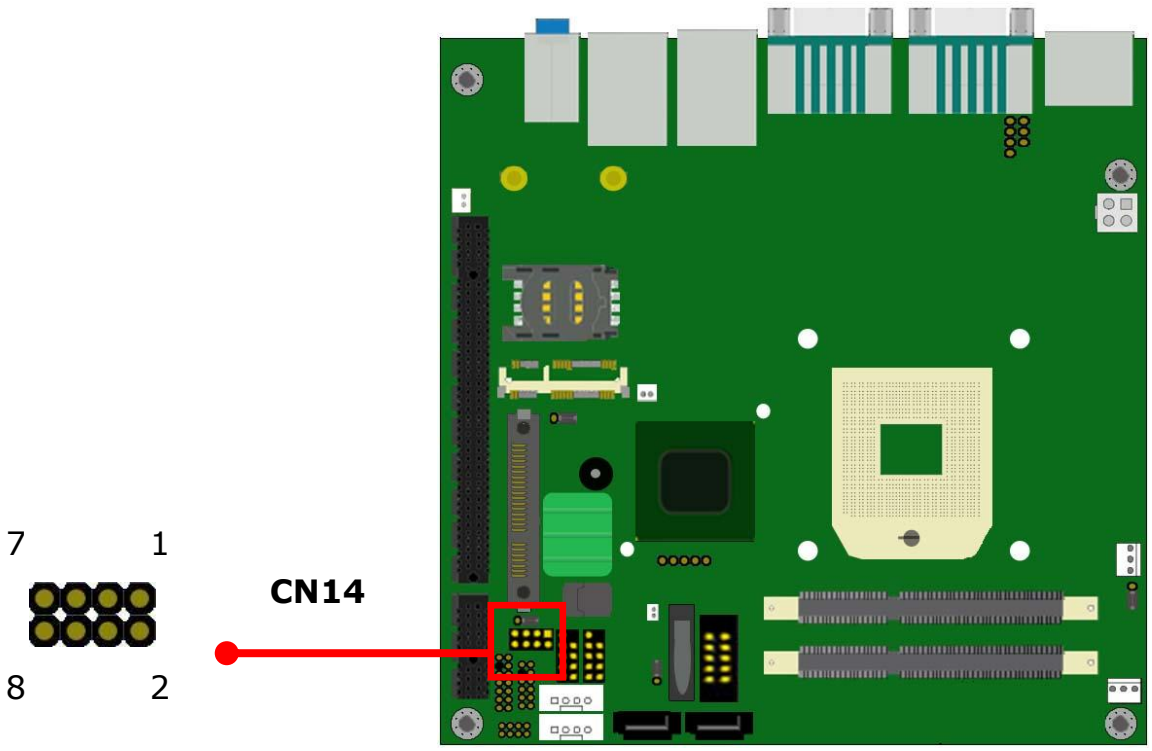
CN11: 2 x 5 header , pitch 2.54 mm			
Pin	**Signal**	**Pin**	**Signal**
1	+5V	2	+5V
3	USB2_ data-	4	USB3_data-
5	USB2_ data+	6	USB3_data+
7	GND	8	GND
9	Key	10	GND

CN12: 2 x 5 header , pitch 2.54 mm			
Pin	**Signal**	**Pin**	**Signal**
1	+5V	2	+5V
3	USB4_ data-	4	USB5_data-
5	USB4_ data+	6	USB5_data+
7	GND	8	GND
9	Key	10	GND



-2.4.7 : CN14 for SPI programmer(Reserve)

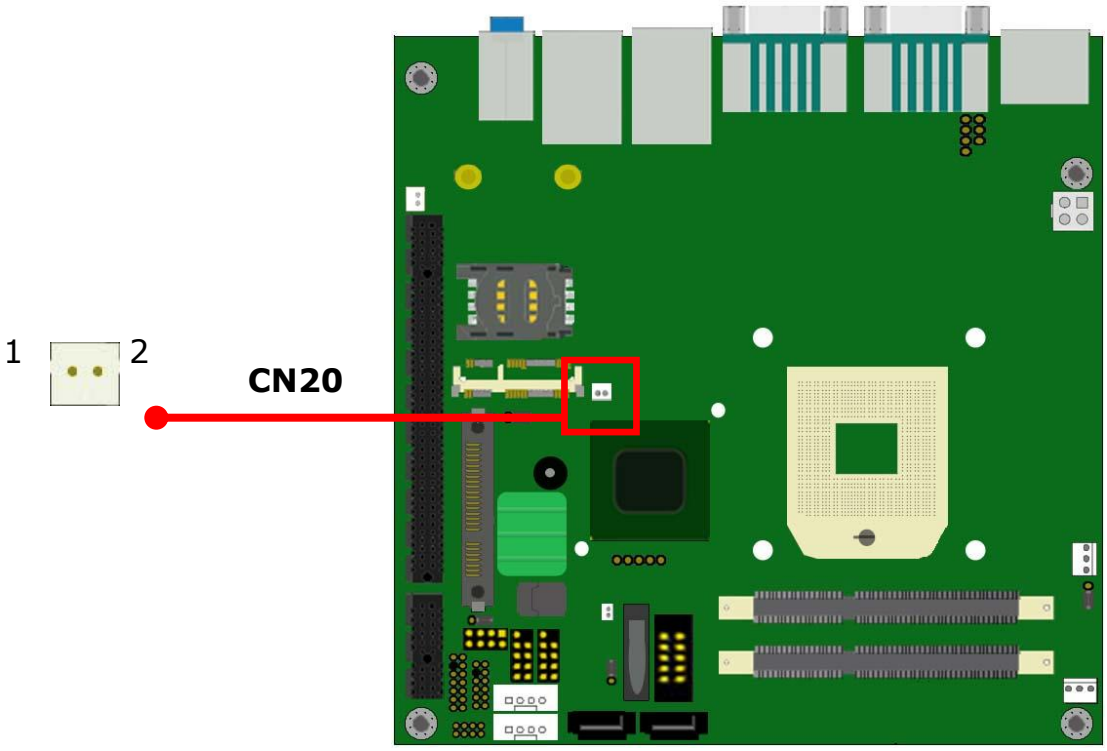
CN14 : 2 x 4 header , pitch 2.54 mm			
Pin	**Signal**	**Pin**	**Signal**
1	+3.3V	2	GND
3	CS_N (Chip Select)	4	SCLK (Serial Clock)
5	MISO (Master Input, Slave Output)	6	MOSI (Master Output, Slave Input)
7	N/C	8	N/C



- 2.4.8 : CN20 for WLAN LED connector for Full-size Mini-PCIe socket

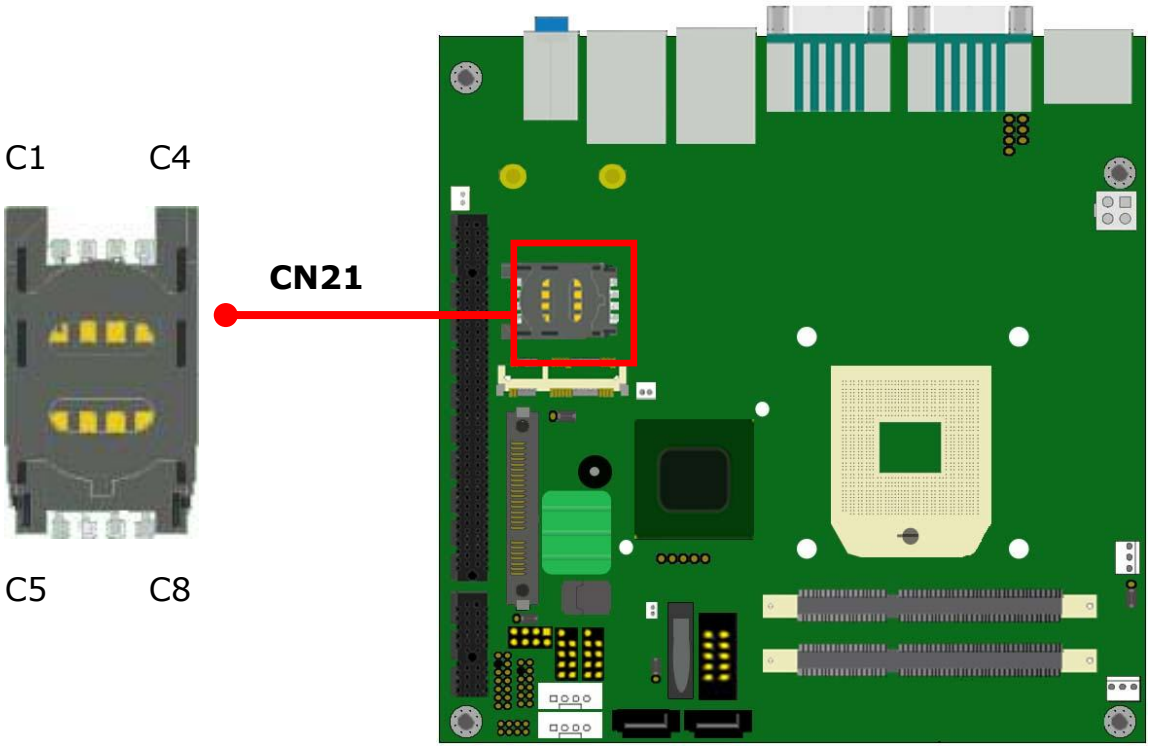
CN20 : 1 x 2 wafer			
Pin	**Signal**	**Pin**	**Signal**
1	LED-	2	+3.3V

Note: Support WLAN / wireless LAN signal



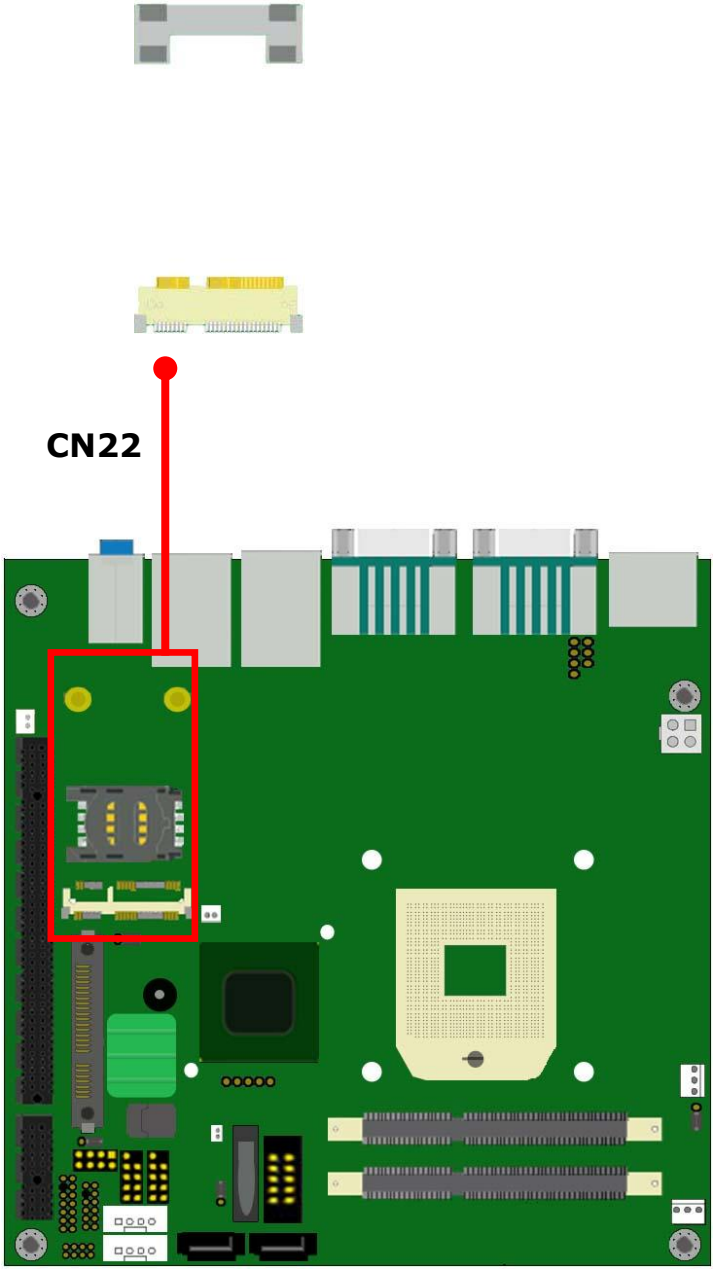
-2.4.9 : CN21 for SIM holder

CN21 : SIM card holder			
Pin	**Signal**	**Pin**	**Signal**
C1	VCC	C2	RESET
C3	CLOCK	C4	Reserved
C5	GND	C6	VPP
C7	I/O	C8	Reserved



- 2.4.10 : CN22 for Full-size Mini-PCIe socket

Pin	Signal	Pin	Signal
1	WAKE	27	GND
2	+3.3V AUX	28	+1.5V
3	N/C	29	GND
4	GND	30	SMBCLK
5	N/C	31	PETN0
6	+1.5V	32	SMBDATA
7	CLKREQ	33	PETP0
8	UIM_PWR	34	GND
9	GND	35	GND
10	UIM_DATA	36	USB_D-
11	REFCLK-	37	GND
12	UIM_CLK	38	USB_D+
13	REFCLK+	39	+3.3V AUX
14	UIM_RESET	40	GND
15	GND	41	+3.3V AUX
16	UIM_VPP	42	LED_WWAN
17	UIM_C8	43	GND
18	GND	44	LED_WLAN
19	UIM_C4	45	N/C
20	W_Disable	46	N/C
21	GND	47	N/C
22	PERST	48	+1.5V
23	PERN0	49	N/C
24	+3.3V AUX	50	GND
25	PERP0	51	N/C
26	GND	52	+3.3V AUX



Note:

Full-size Mini-PCIe card could support USB + SATA or USB + PCIE signal.

The default setting is set as USB + PCIE signal.

Please into BIOS and select SATA or PCIE signal to match your device.

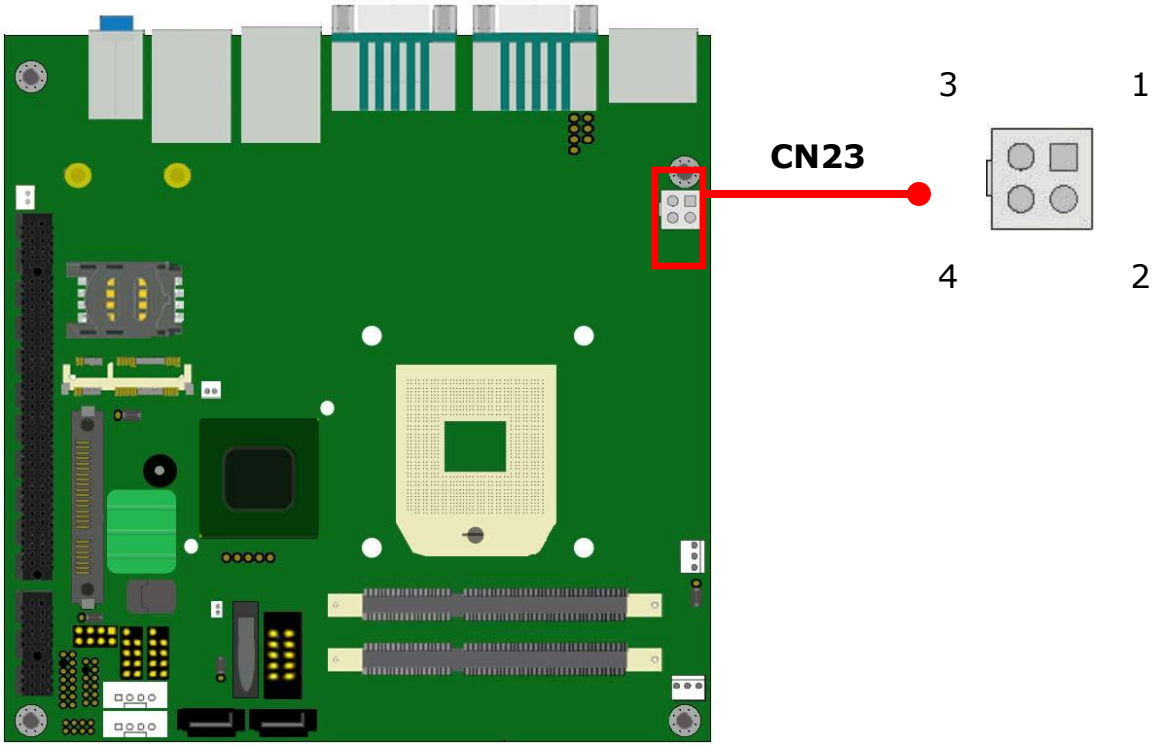
For example :

Please into BIOS and set ” SATA ” when you install a Full-size add-on card, such as mSATA SSD...

Please into BIOS and set ” PCIE ” when you install a Full-size add-on card, such as WIFI card....

-2.4.11 : CN23 for internal 4-pin power input

CN23 : ATX 2 x 2			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GND
3	8V ~ 32V DC input	4	8V ~ 32V DC input

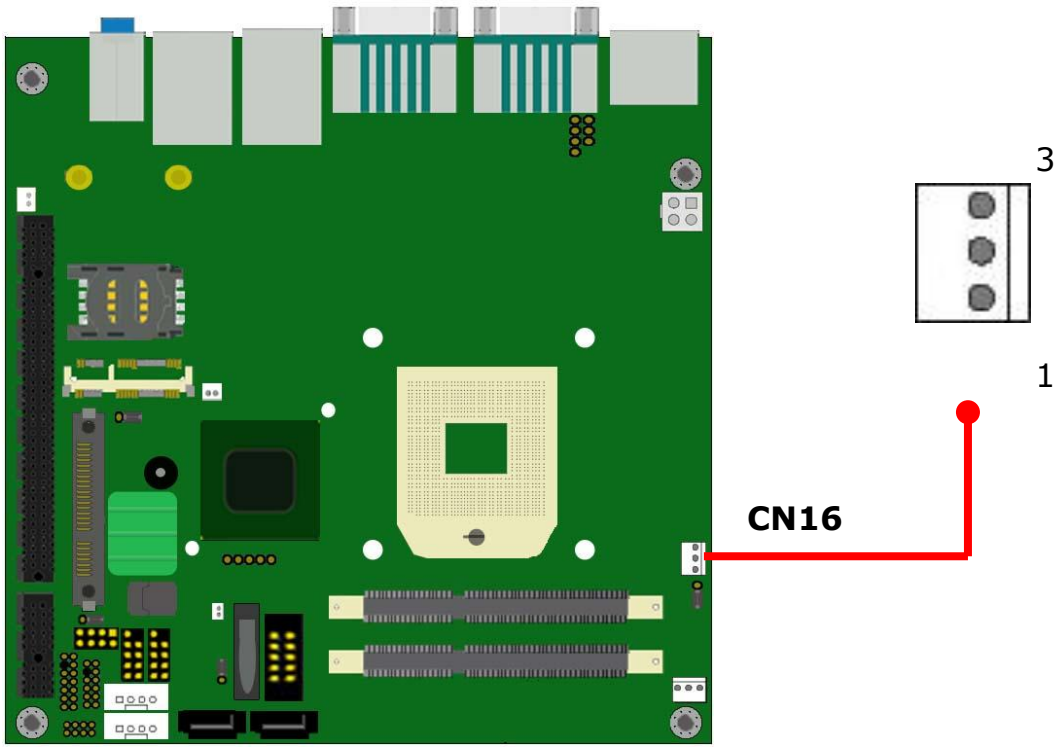


-2.4.12 : CN7 for system Fan connector

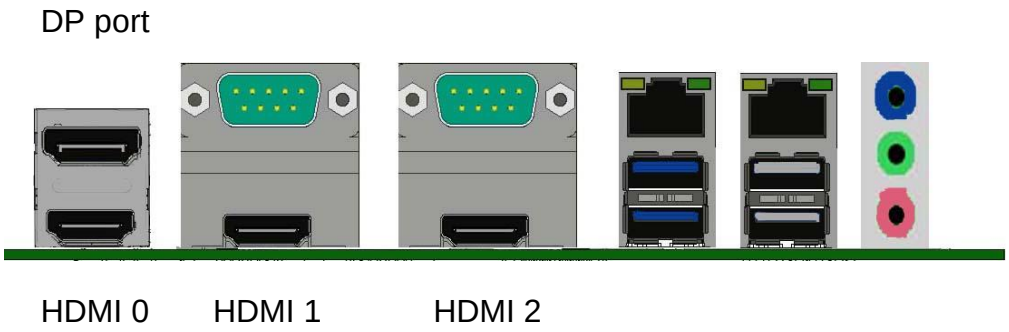
CN7 : 1 x 3 wafer			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+12V
3	Sense		

CN16 for CPU Fan connector

CN16: 1 x 3 wafer			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	+12V
3	Sense		



-2.5 : Triple Display application note :



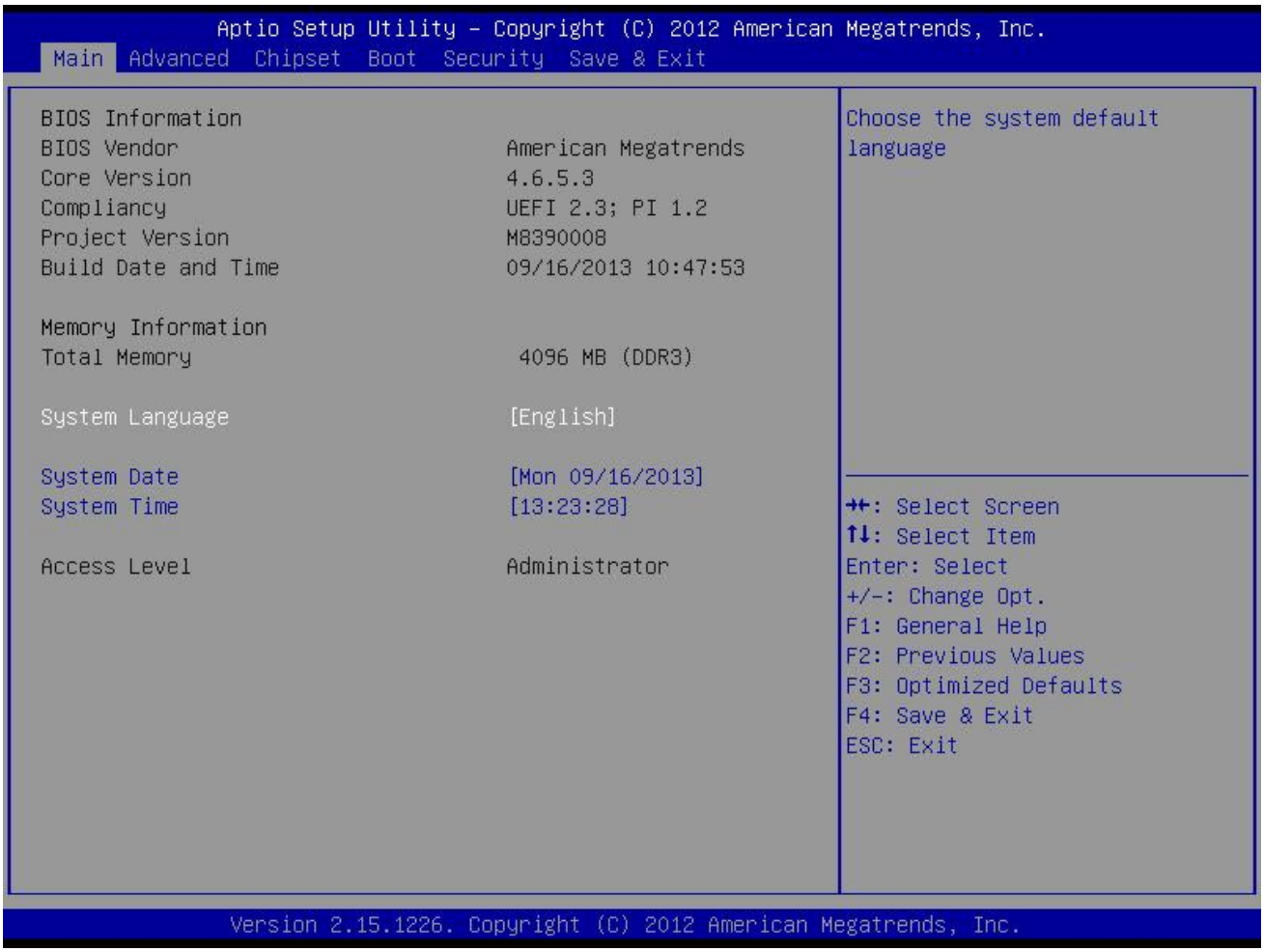
HDMI 0 + HDMI 1 + HDMI 2 = Pass
HDMI 0 + HDMI 1 + DP port = Fail
HDMI 0 + HDMI 2 + DP port = Pass
HDMI 1 + HDMI 2 + DP port = Pass

Note: If need to connect with DP port for triple display application, the HDMI 2 must be used in the configuration, Otherwise, the system will show two display only.

3. BIOS setting Menu

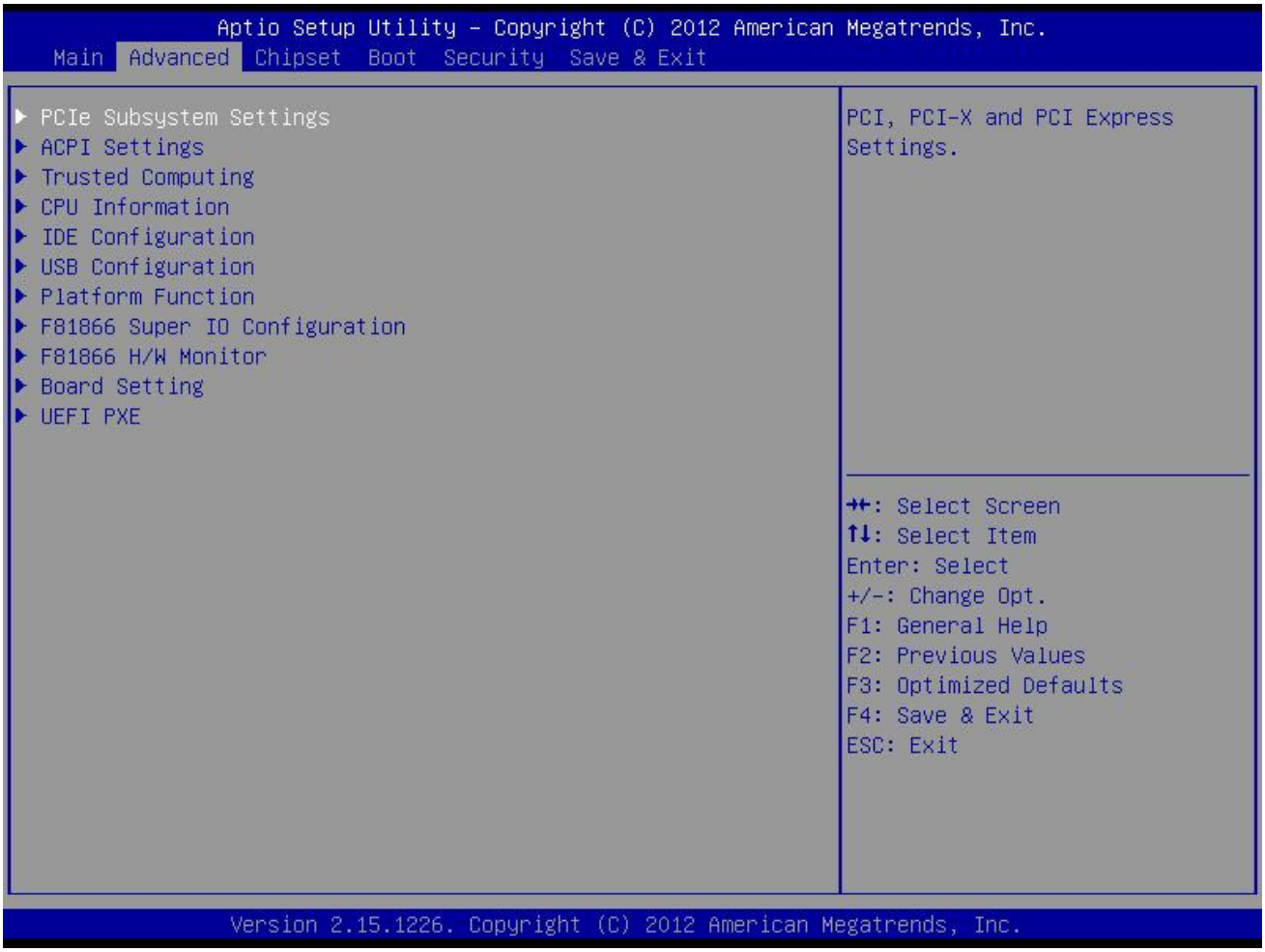
- 3.1 Main Menu

The Main Menu of BIOS Setup Utility provide a quick overview of basic system information and the ability to change the system Date, time ……..


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
BIOS Information
BIOS Vendor American Megatrends
Core Version 4.6.5.3
Compliancy UEFI 2.3; PI 1.2
Project Version M8390008
Build Date and Time 09/16/2013 10:47:53
Memory Information
Total Memory 4096 MB (DDR3)
System Language [English]
System Date [Mon 09/16/2013]
System Time [13:23:28]
Access Level Administrator
Choose the system default language
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.2 Advanced Menu

The Advanced Menu of BIOS Setup Utility allows users to configure advanced system settings.

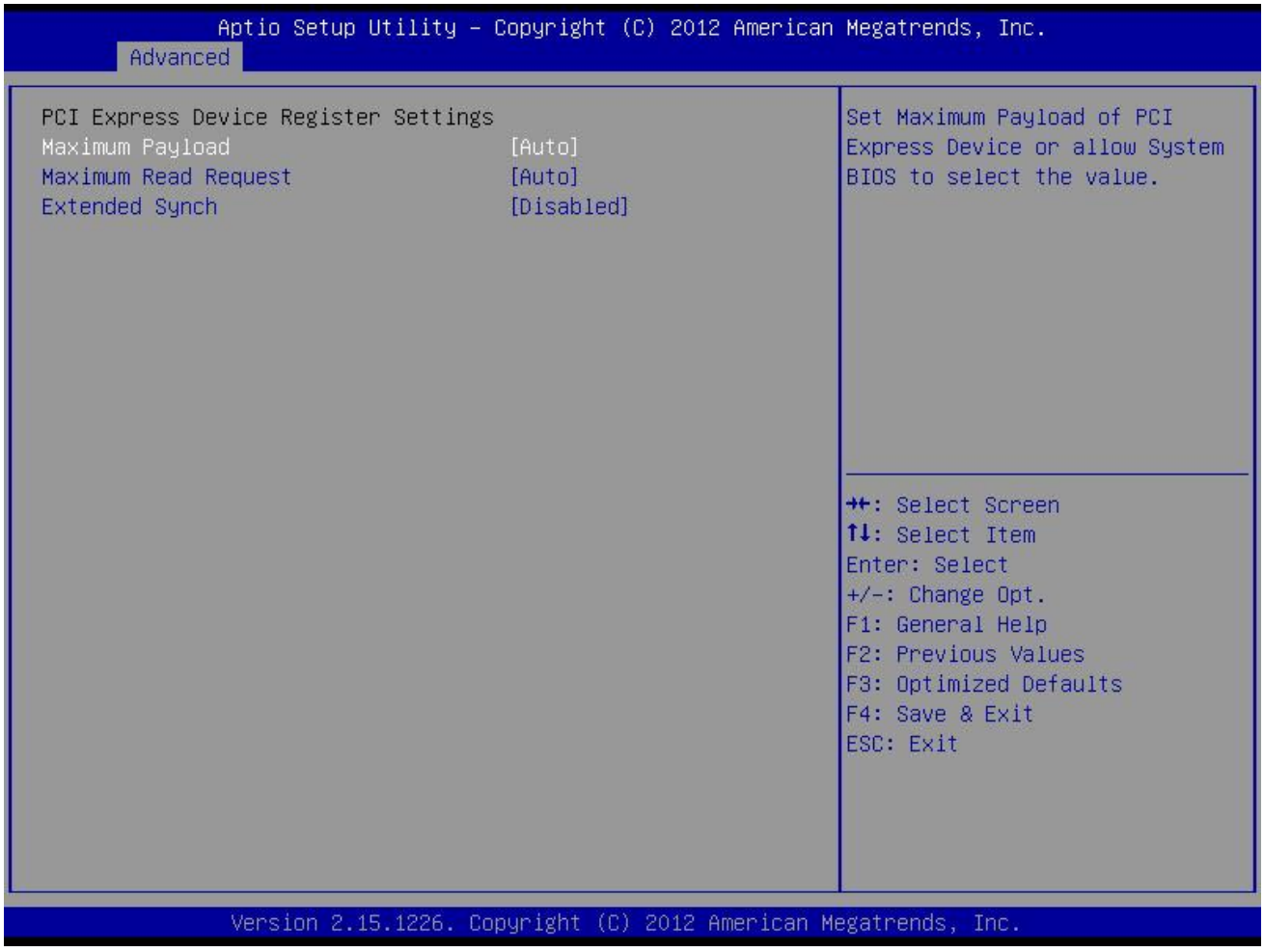


- 3.2.1 Advanced Menu

PCIe Subsystem Setting:

Maximum Read Request < Auto >

Description: This item manually sets the maximum read request size of the PCI Express device or allows the system BIOS to choose the value (Auto). The options are Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes and 4096 Bytes.

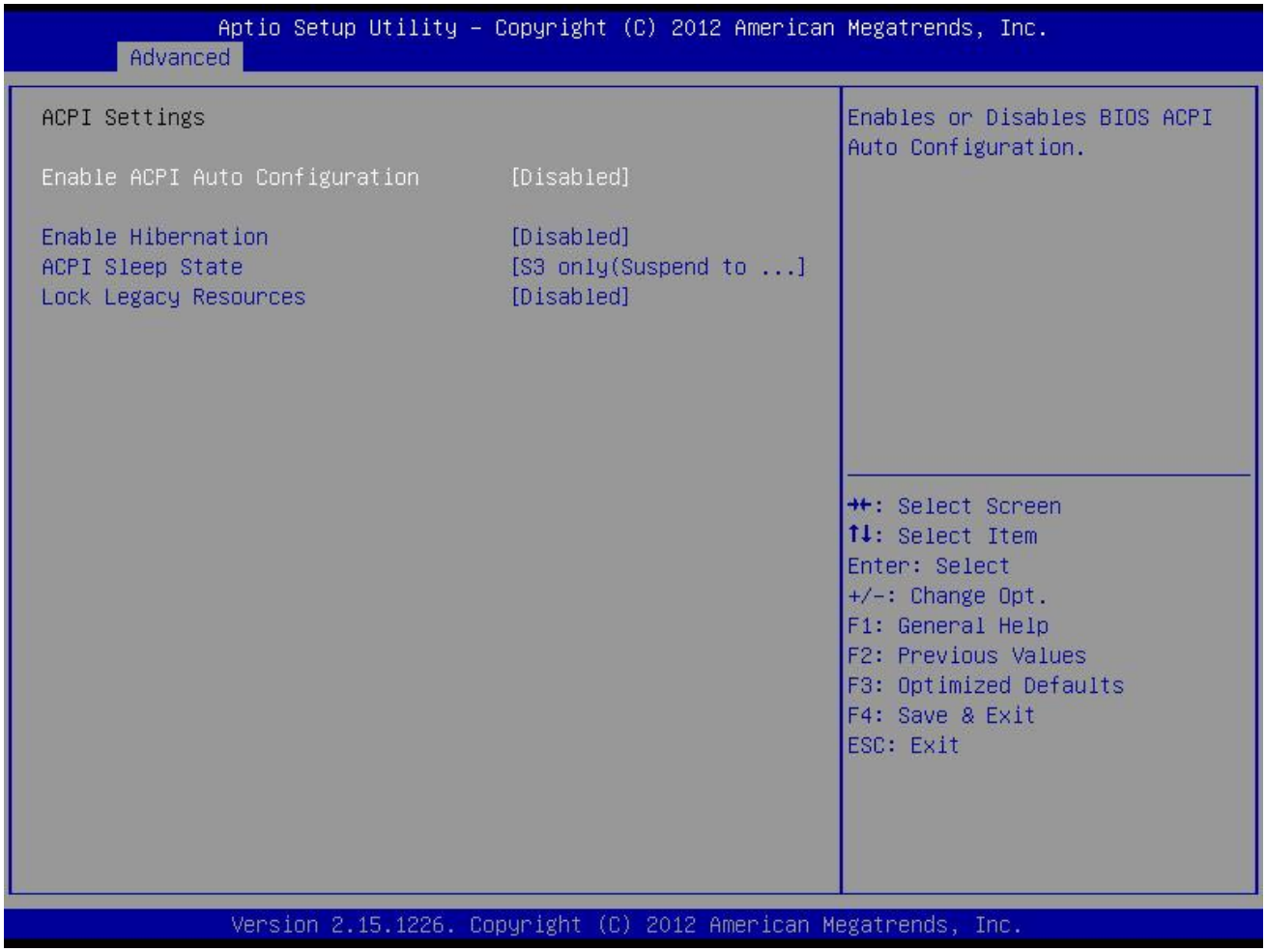

Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
PCI Express Device Register Settings
Maximum Payload [Auto]
Maximum Read Request [Auto]
Extended Synch [Disabled]
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.2.2 Advanced Menu

ACPI Setting:

Enable ACPI Auto Configuration < Disable >

Description : Use this feature to configure Advanced Configuration and Power Interface (ACPI) power management settings for your system.

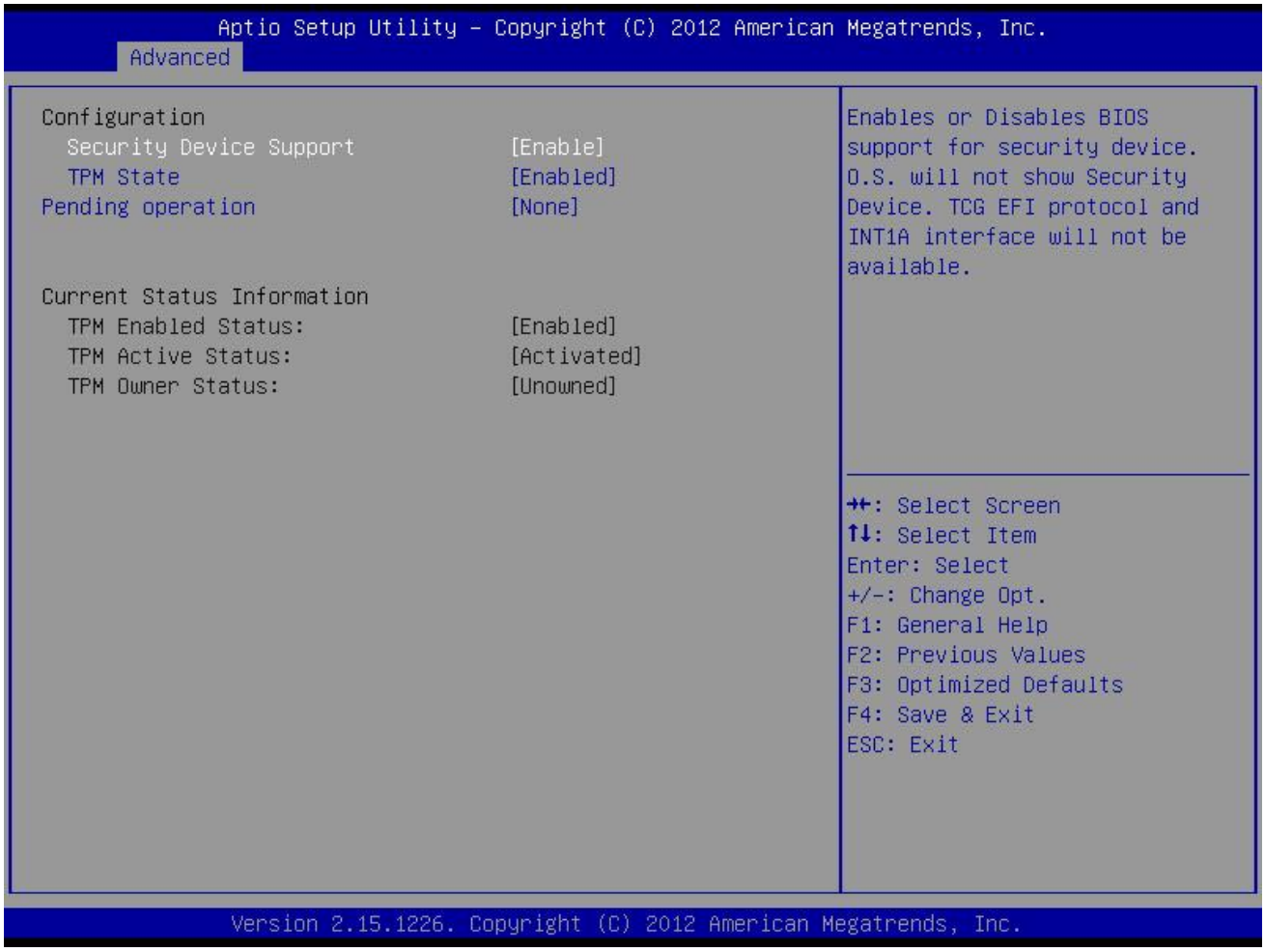

Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
ACPI Settings
Enable ACPI Auto Configuration [Disabled]
Enable Hibernation [Disabled]
ACPI Sleep State [S3 only(Suspend to ...]
Lock Legacy Resources [Disabled]
Enables or Disables BIOS ACPI Auto Configuration.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.2.3 Advanced Menu

Trsuted Computing:

TPM State *< Enable >*

Description : Select Enabled to activate support for trusted platforms (TPM 1.1/1.2) and allow the BIOS to automatically download the drivers needed to provide support for the platforms specified. The options are Disable and Enable. >

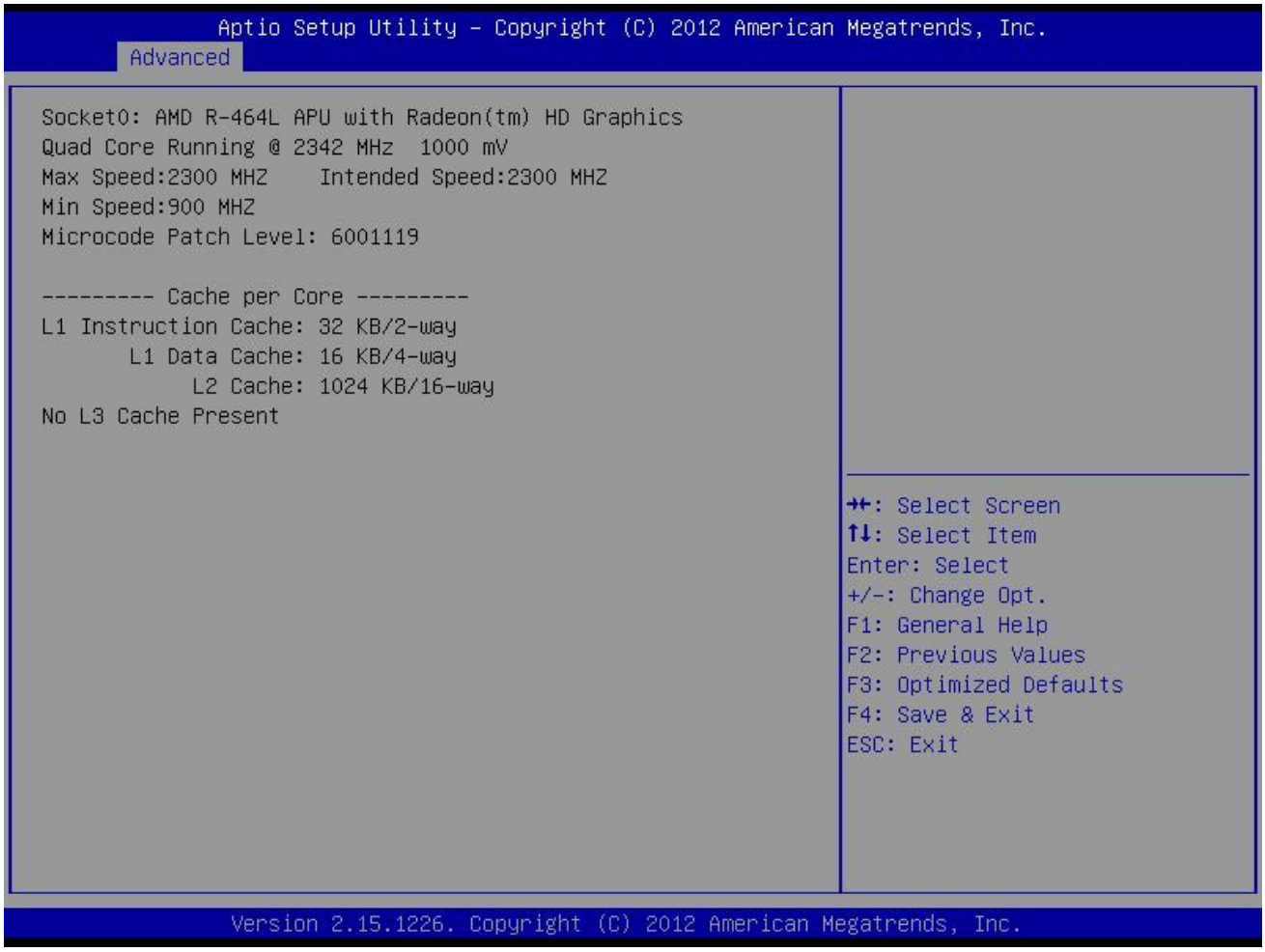

Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
Configuration
Security Device Support [Enable]
TPM State [Enabled]
Pending operation [None]
Current Status Information
TPM Enabled Status: [Enabled]
TPM Active Status: [Activated]
TPM Owner Status: [Unowned]
Enables or Disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.2.4 Advanced Menu

CPU Information:

This item displays the current CPU Revision, Current CPU1 Memory Frequency, Memory Type and Memory Reference Code Revision.

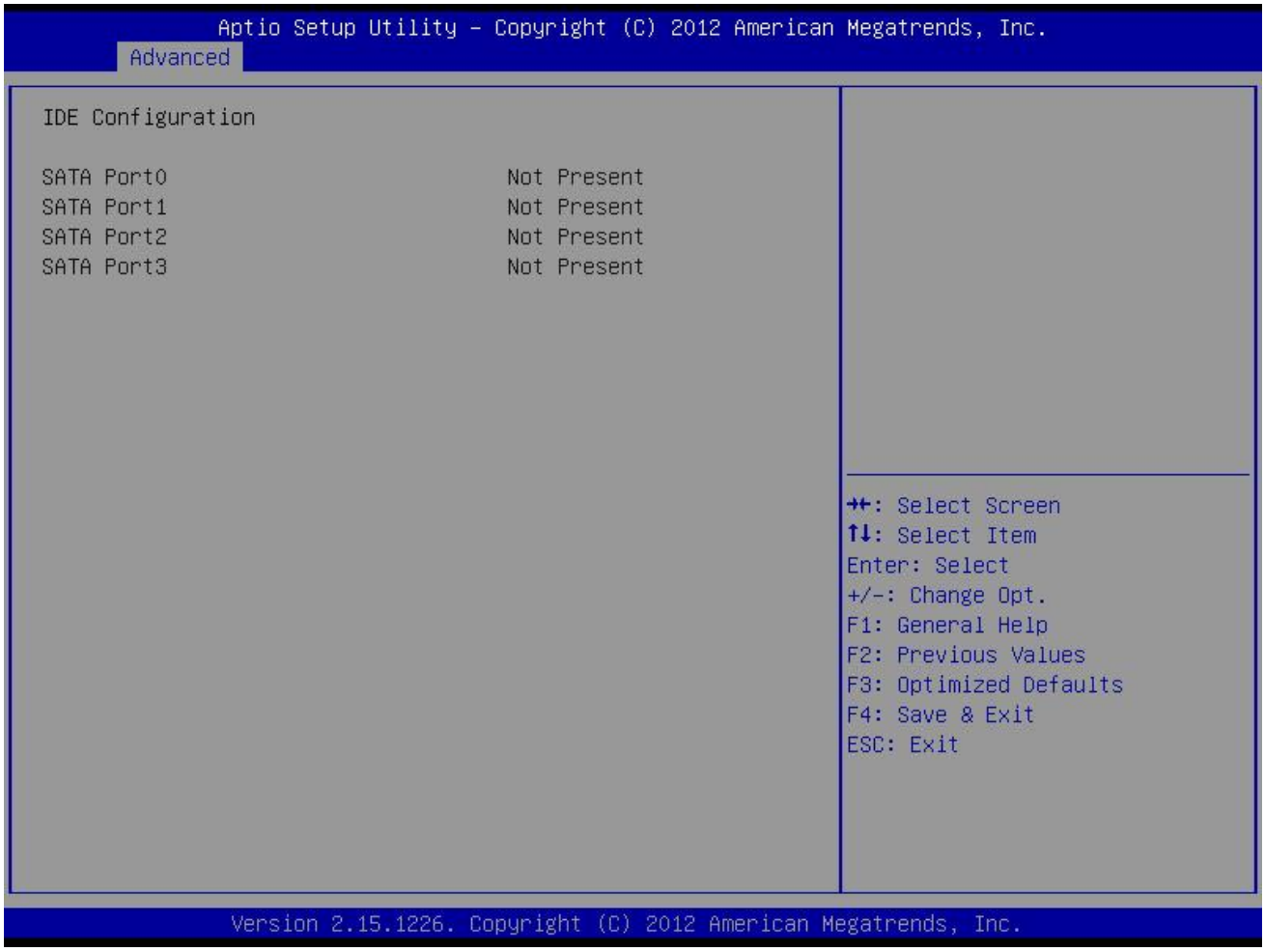
Description : This item displays the current CPU information."


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
Socket0: AMD R-464L APU with Radeon(tm) HD Graphics
Quad Core Running @ 2342 MHz 1000 mV
Max Speed:2300 MHZ Intended Speed:2300 MHZ
Min Speed:900 MHZ
Microcode Patch Level: 6001119
--------- Cache per Core ---------
L1 Instruction Cache: 32 KB/2-way
L1 Data Cache: 16 KB/4-way
L2 Cache: 1024 KB/16-way
No L3 Cache Present
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.2.5 Advanced Menu

IDE Configuration:

Description : When this submenu is selected, the AMI BIOS automatically detects the presence of the IDE Devices and displays the following items:



- 3.2.6 Advanced Menu

F81866 Super IO Configuration:

Description : Select Enabled to enable the onboard serial port. The options are Enabled and Disabled.

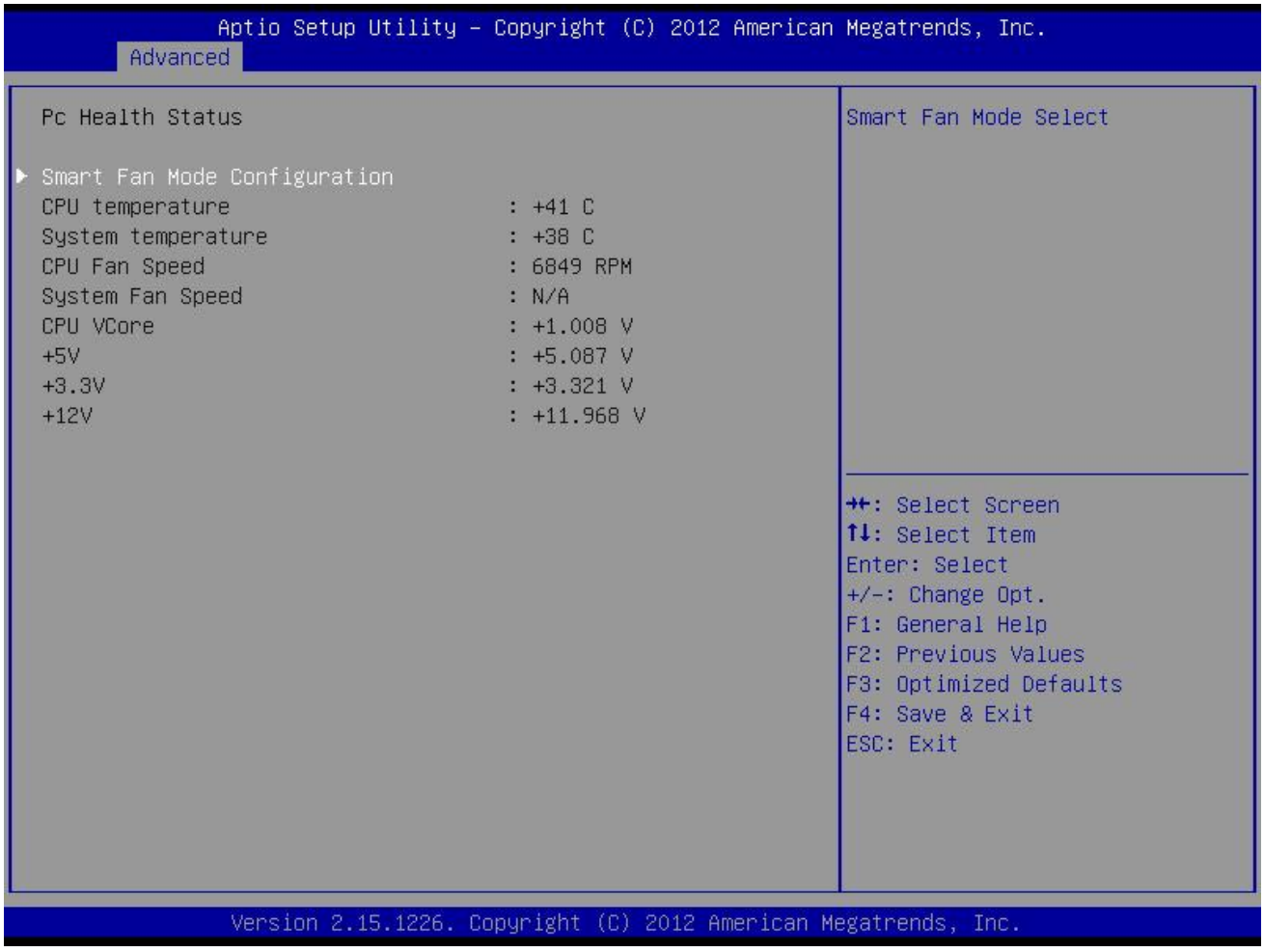
Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
F81866 Super IO Configuration
F81866 Super IO Chip F81866
Serial Port 0 Configuration
Serial Port 1 Configuration
Serial Port 2 Configuration
Set Parameters of Serial Port 0 (COMA)
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.2.7 Advanced Menu

F81866 H/W monitor:

PC Health Status *< Enabled/Disabled >*

Description : This feature allows the user to check CPU temperature and the fan speed. And also displays the current voltages of the above voltage monitors


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Advanced
Pc Health Status
Smart Fan Mode Configuration
CPU temperature : +41 C
System temperature : +38 C
CPU Fan Speed : 6849 RPM
System Fan Speed : N/A
CPU VCore : +1.008 V
+5V : +5.087 V
+3.3V : +3.321 V
+12V : +11.968 V
Smart Fan Mode Select
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

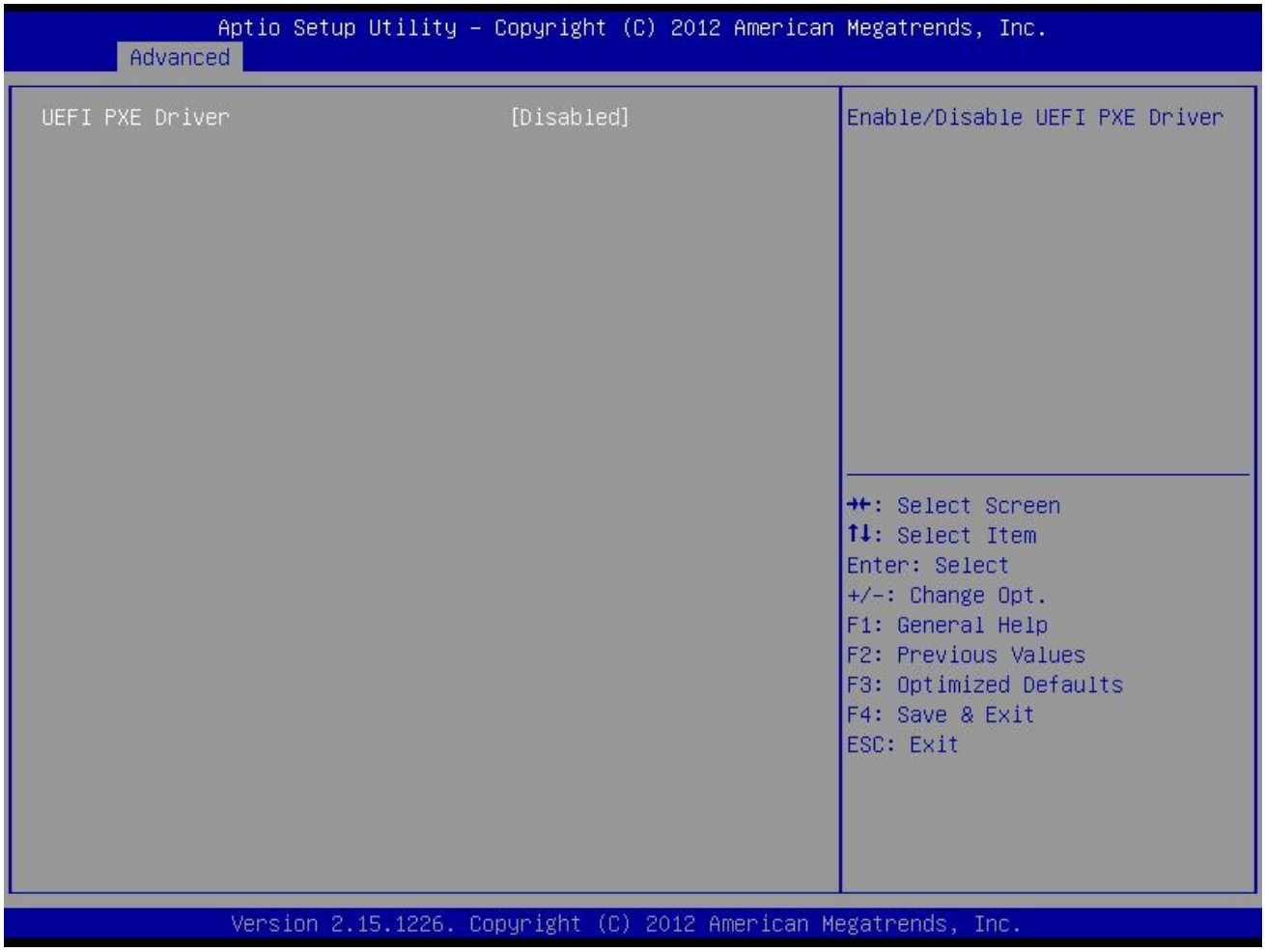
- 3.2.8 Advanced Menu

UEFI PXE:

UEFI PXE Driver *< Enabled/Disabled >*

Select Enabled to enable the capability to 'wake-up' the system from the S5~power state (Soft Off State) through the Ethernet controller. The settings are Enabled and Disabled.

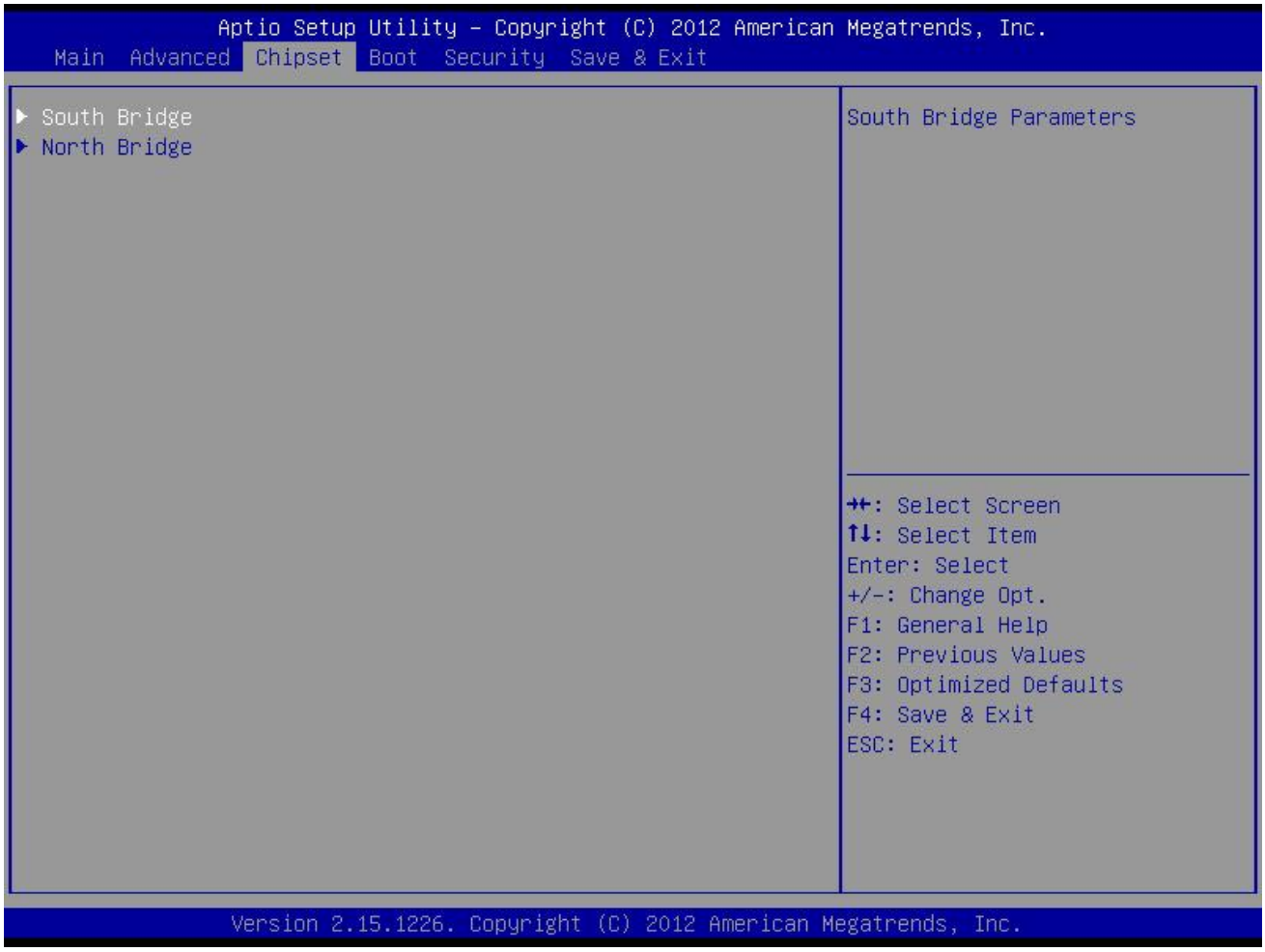
Select Enabled to enable on board AMD LAN device PXE remote boot function



- 3.3 Chipset Menu

Chipset:

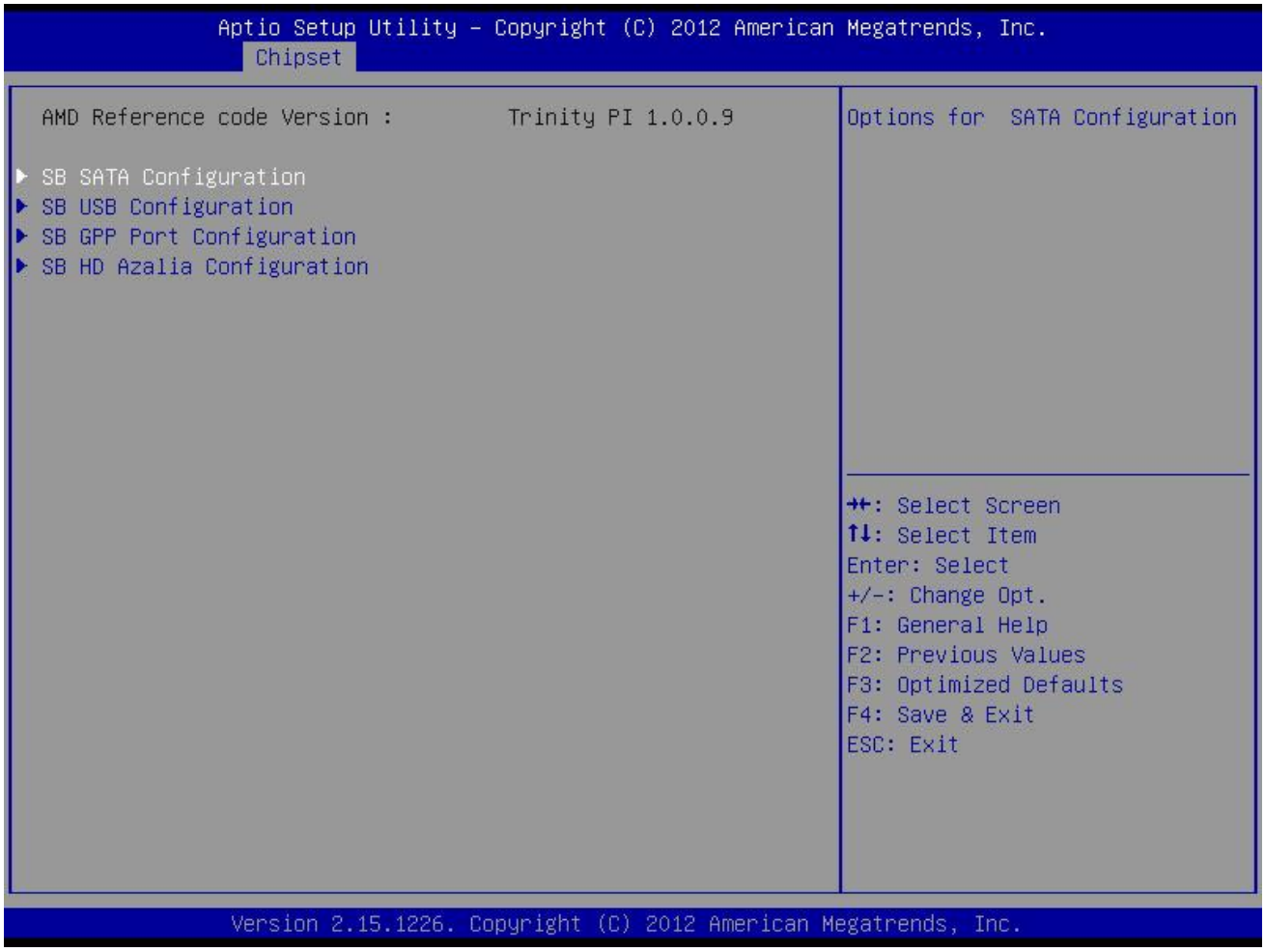
Description : South Bridge & North Bridge Setting



- 3.3.1 Chipset Menu

AMD Reference code version :

Description: Check the code version and optional for SATA, USB and audio function.



- 3.3.2 Chipset Menu

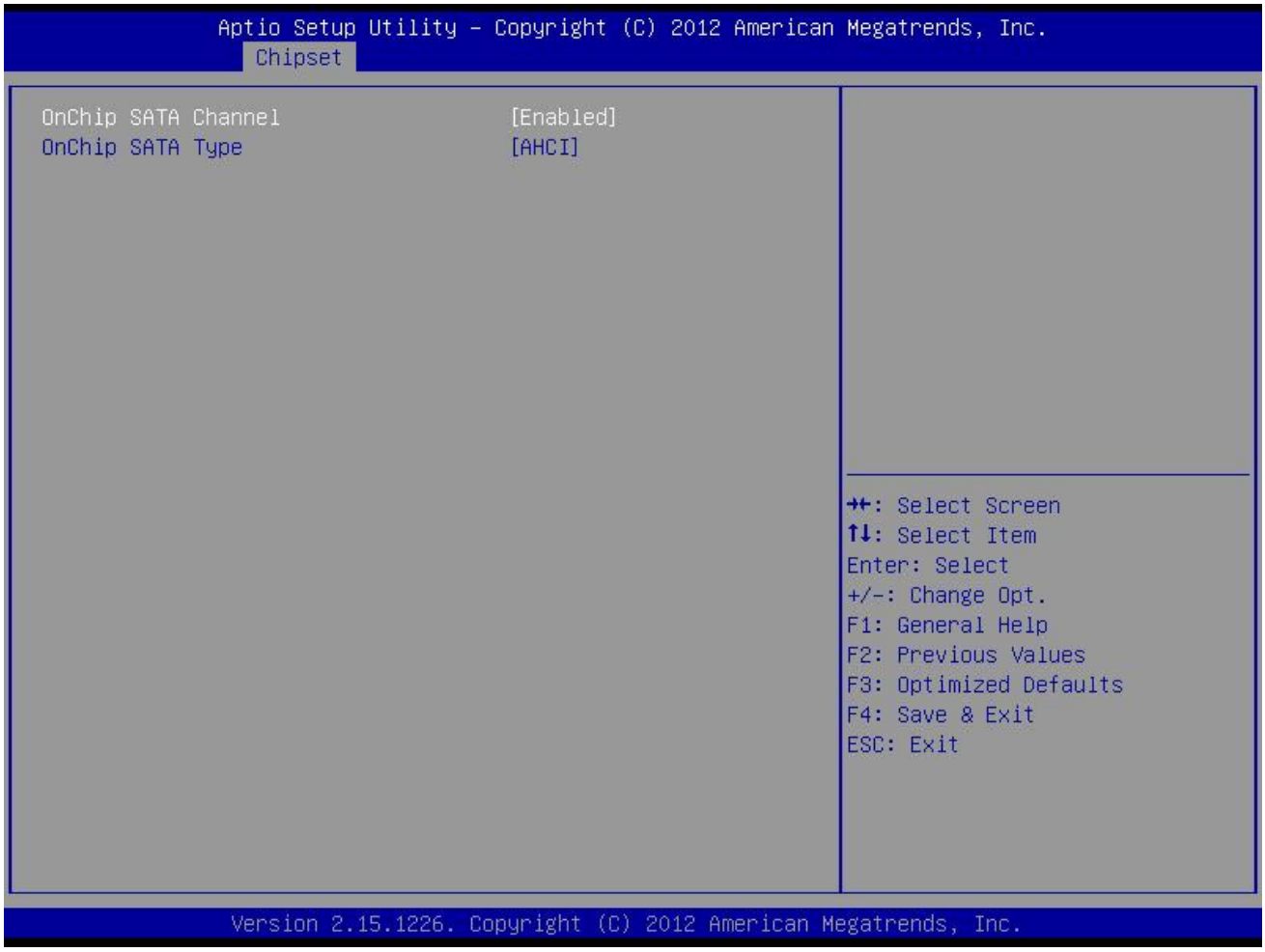
South Bridge:

OnChip SATA channel *< Disabled/enabled >*

Description: Customer could enabled/disabled SATA function here.

Default setting is <Enabled>

Onchip SATA Type selects the mode for the installed drives. The options are Disabled, IDE Mode, AHCI Mode and RAID Mode. Default setting is <AHCI>



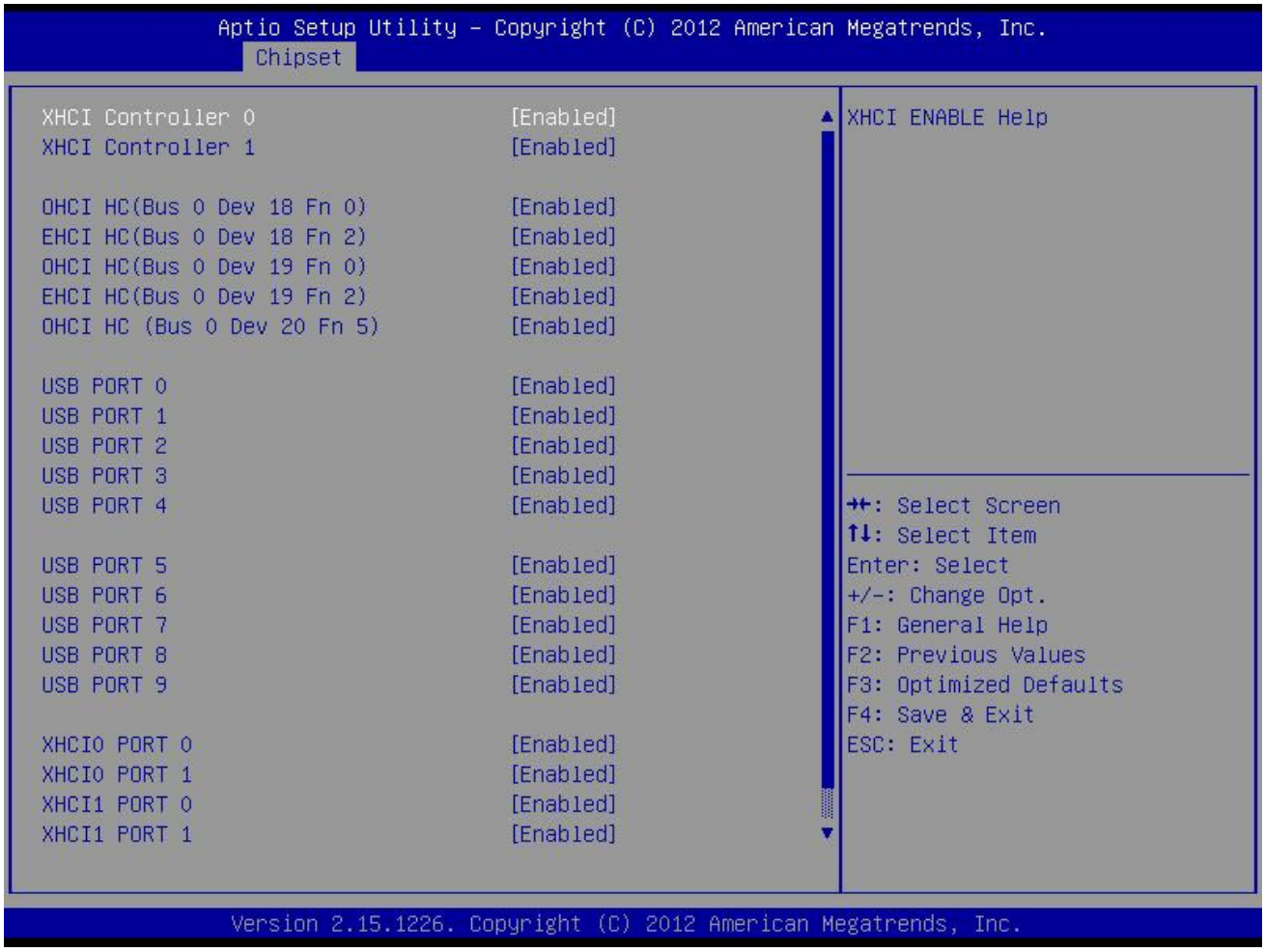
- 3.3.3 Chipset Menu

SB USB Configuration:

XHCI Controller 0/1 < Disabled/enabled >

Description: This feature enables support for USB function parameters The options are Enabled, and Disabled.

Default setting is <Enabled>

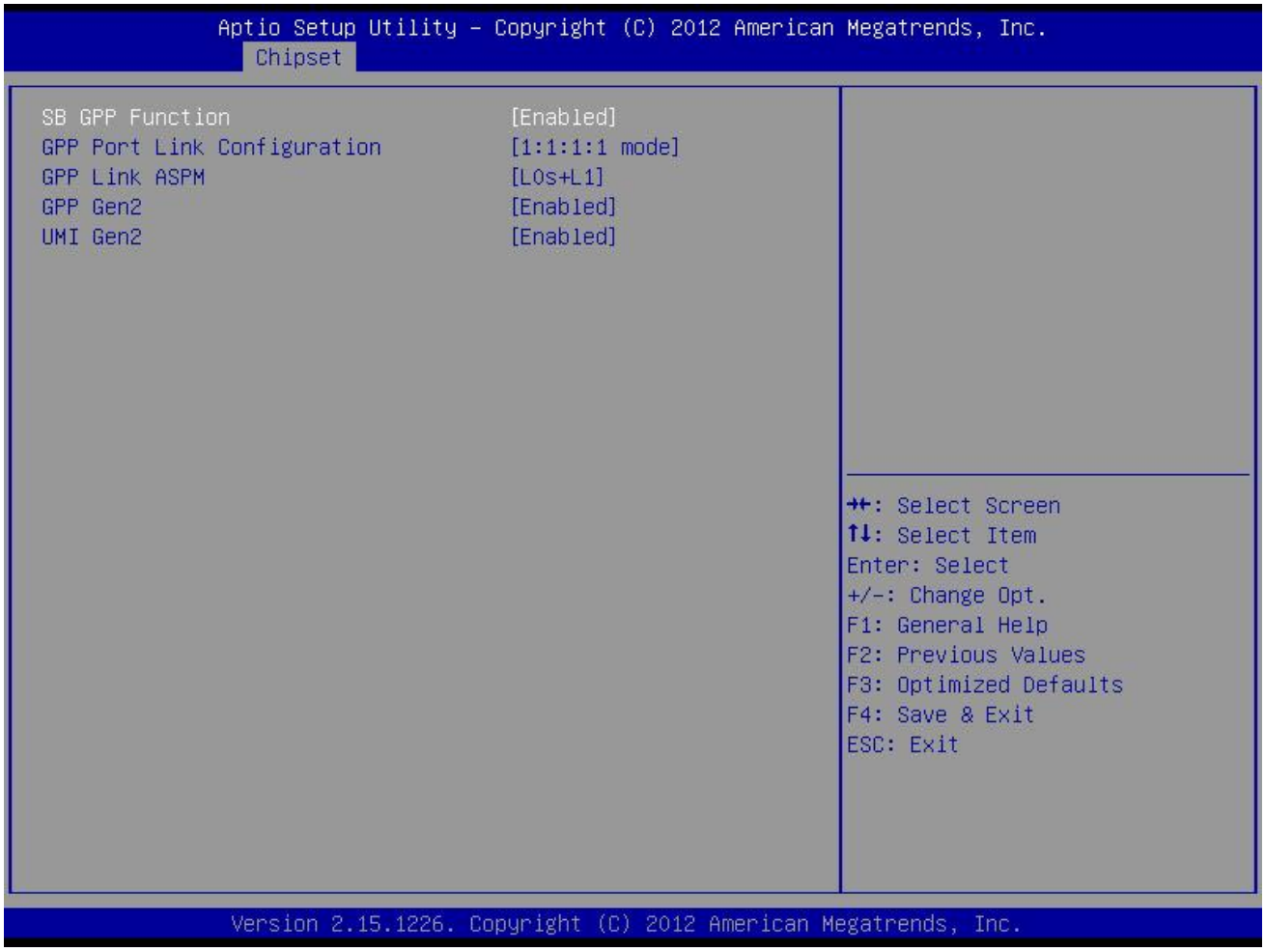

Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
XHCI Controller 0 [Enabled]
XHCI Controller 1 [Enabled]
OHCI HC(Bus 0 Dev 18 Fn 0) [Enabled]
EHCI HC(Bus 0 Dev 18 Fn 2) [Enabled]
OHCI HC(Bus 0 Dev 19 Fn 0) [Enabled]
EHCI HC(Bus 0 Dev 19 Fn 2) [Enabled]
OHCI HC (Bus 0 Dev 20 Fn 5) [Enabled]
USB PORT 0 [Enabled]
USB PORT 1 [Enabled]
USB PORT 2 [Enabled]
USB PORT 3 [Enabled]
USB PORT 4 [Enabled]
USB PORT 5 [Enabled]
USB PORT 6 [Enabled]
USB PORT 7 [Enabled]
USB PORT 8 [Enabled]
USB PORT 9 [Enabled]
XHCIO PORT 0 [Enabled]
XHCIO PORT 1 [Enabled]
XHCI1 PORT 0 [Enabled]
XHCI1 PORT 1 [Enabled]
XHCI ENABLE Help
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.3.4 Chipset Menu

SB GPP port configuration:

SB GPP Function *< Disabled/enabled >*

Description:

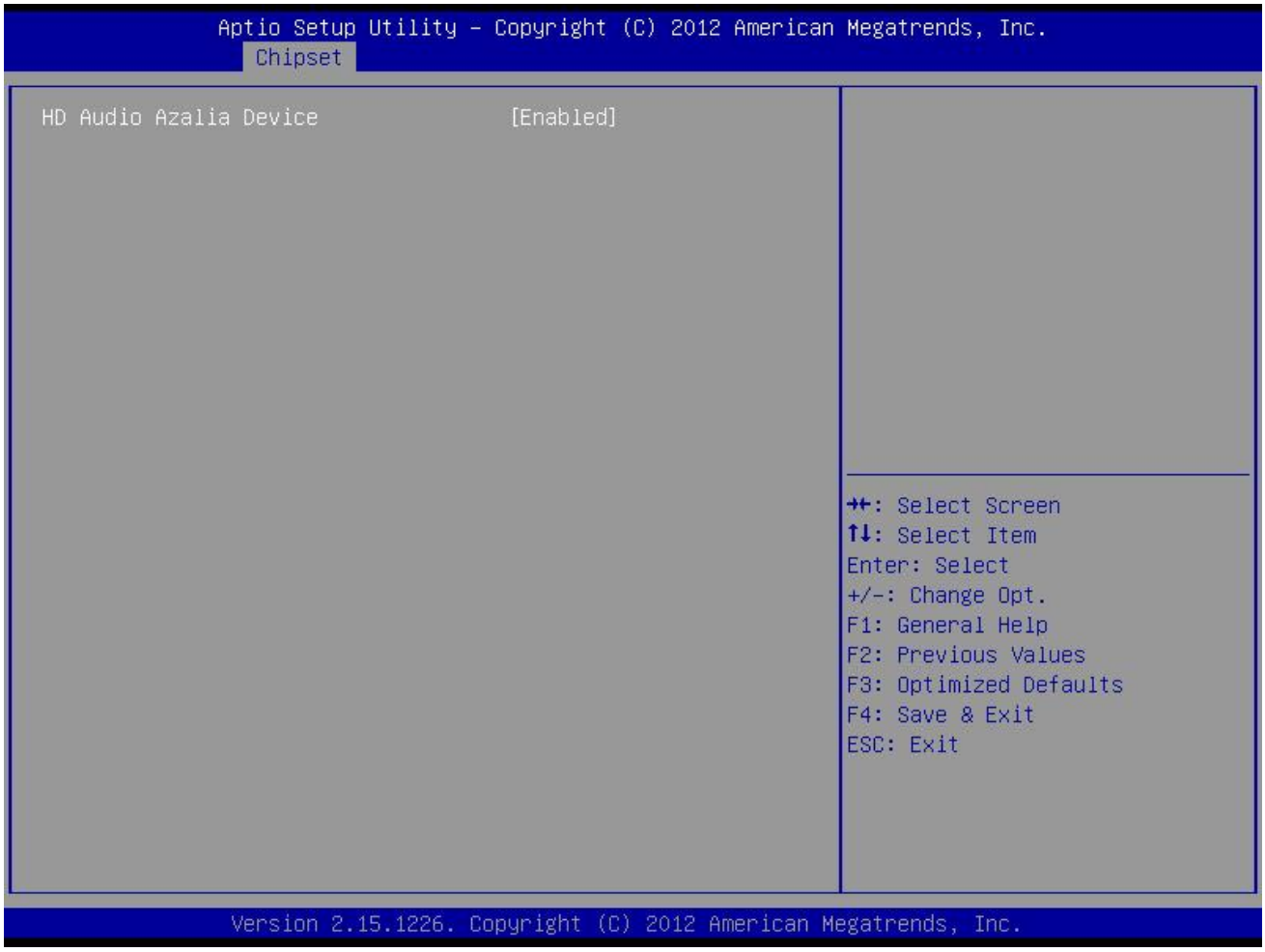


- 3.3.5 Chipset Menu

SB HD Azalia configuration:

HD Audio Azalia Device < Disabled/enabled >

Description: Select Enabled to enable the Azalia High Definition Audio feature. The settings are Enabled and Disabled.
Default setting is <Enabled>



- 3.3.6 Chipset Menu

North Bridge:

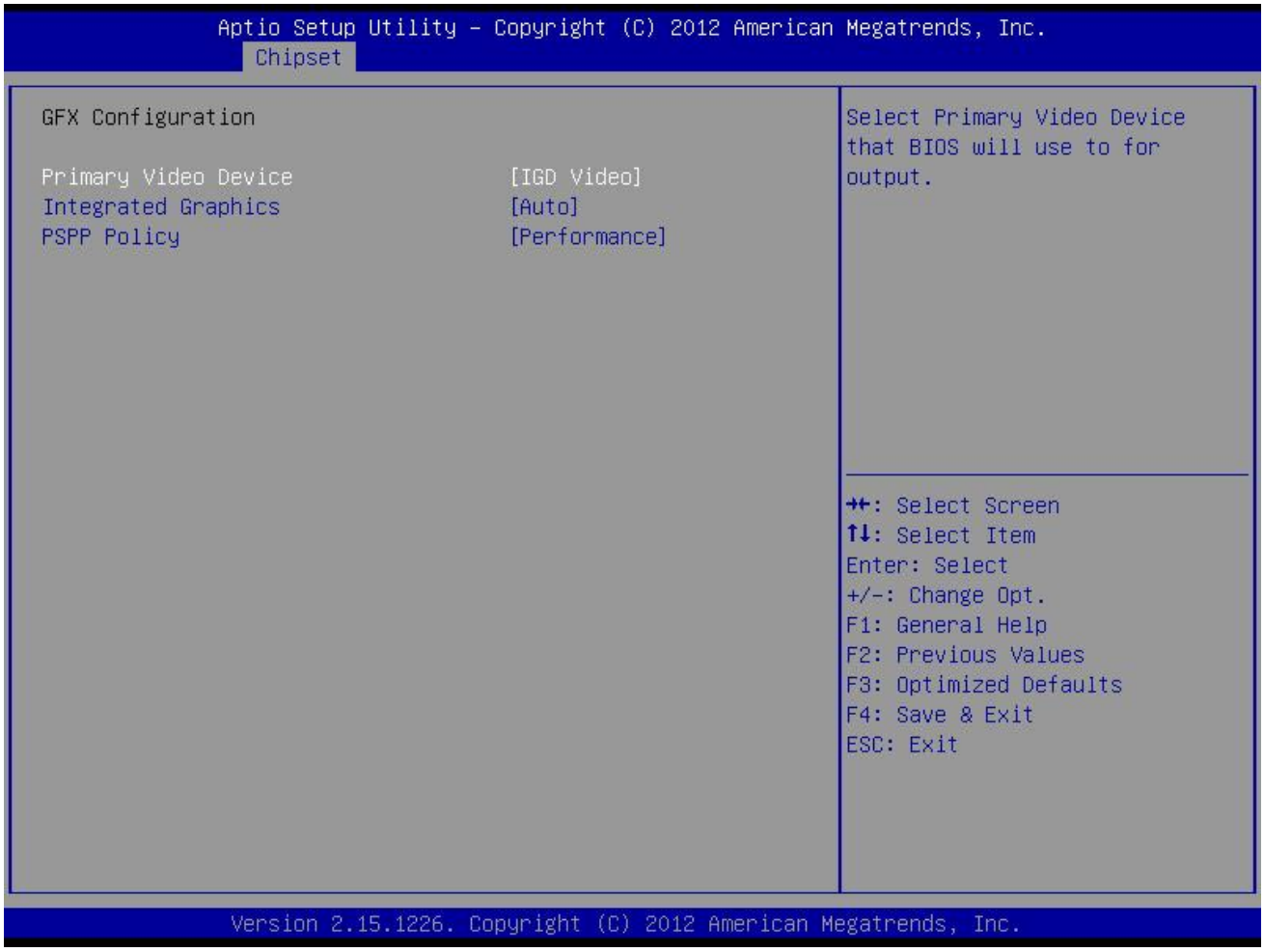
Primary Video Device *< IGD Video >*

Description: Select primary video device that BIOS will use to for output

Default setting is <IGT Video>

IGT : Integrated Graphics Device.

PEG : PCI Express Graphics


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
GFX Configuration
Primary Video Device [IGD Video]
Integrated Graphics [Auto]
PSPP Policy [Performance]
Select Primary Video Device that BIOS will use to for output.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

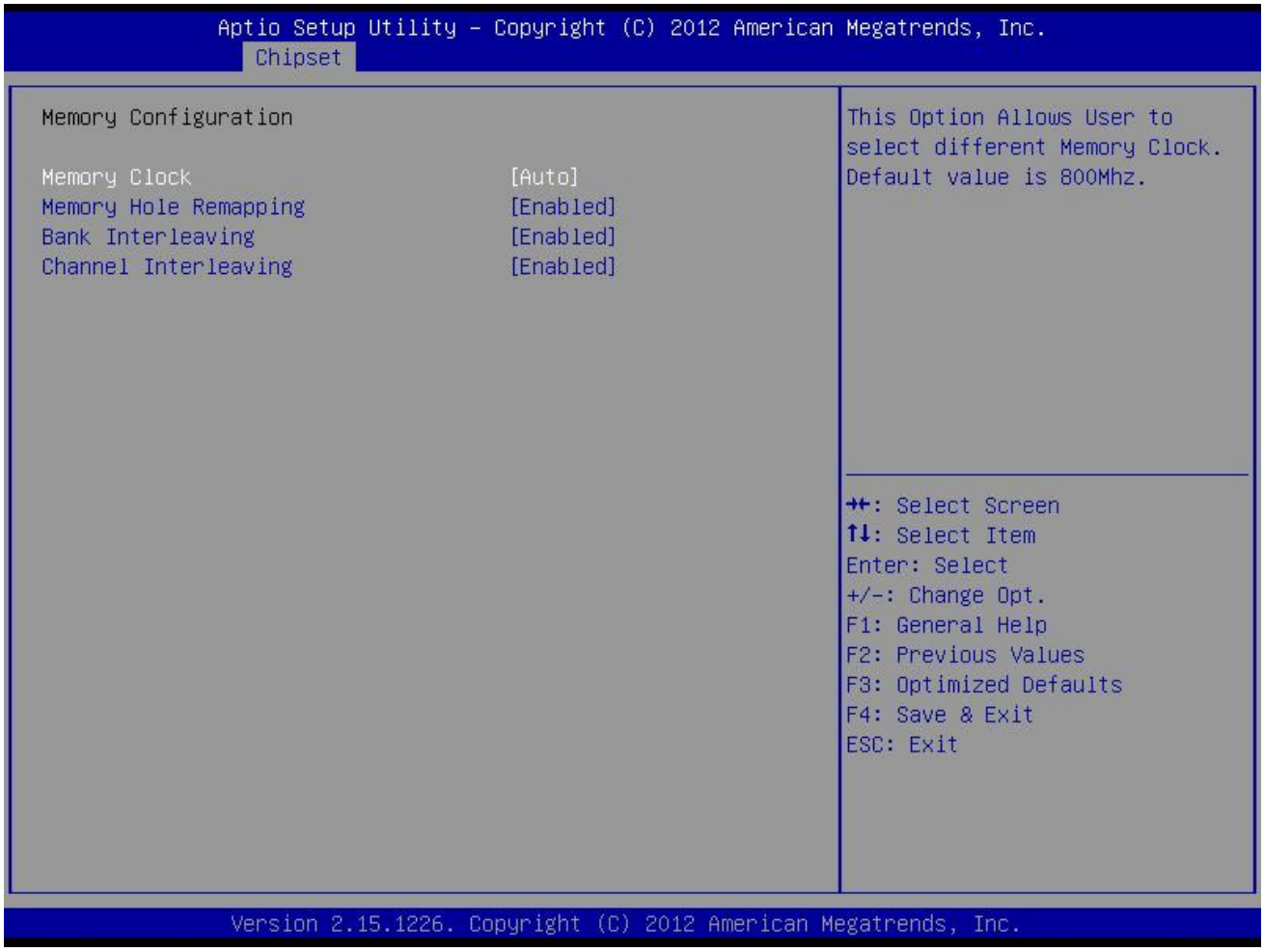
- 3.3.7 Chipset Menu

Memory Configuration:

Memory Clock *< Auto >*

Description: This feature allows the user to select the memory speed. Under normal conditions, please set this to Auto.

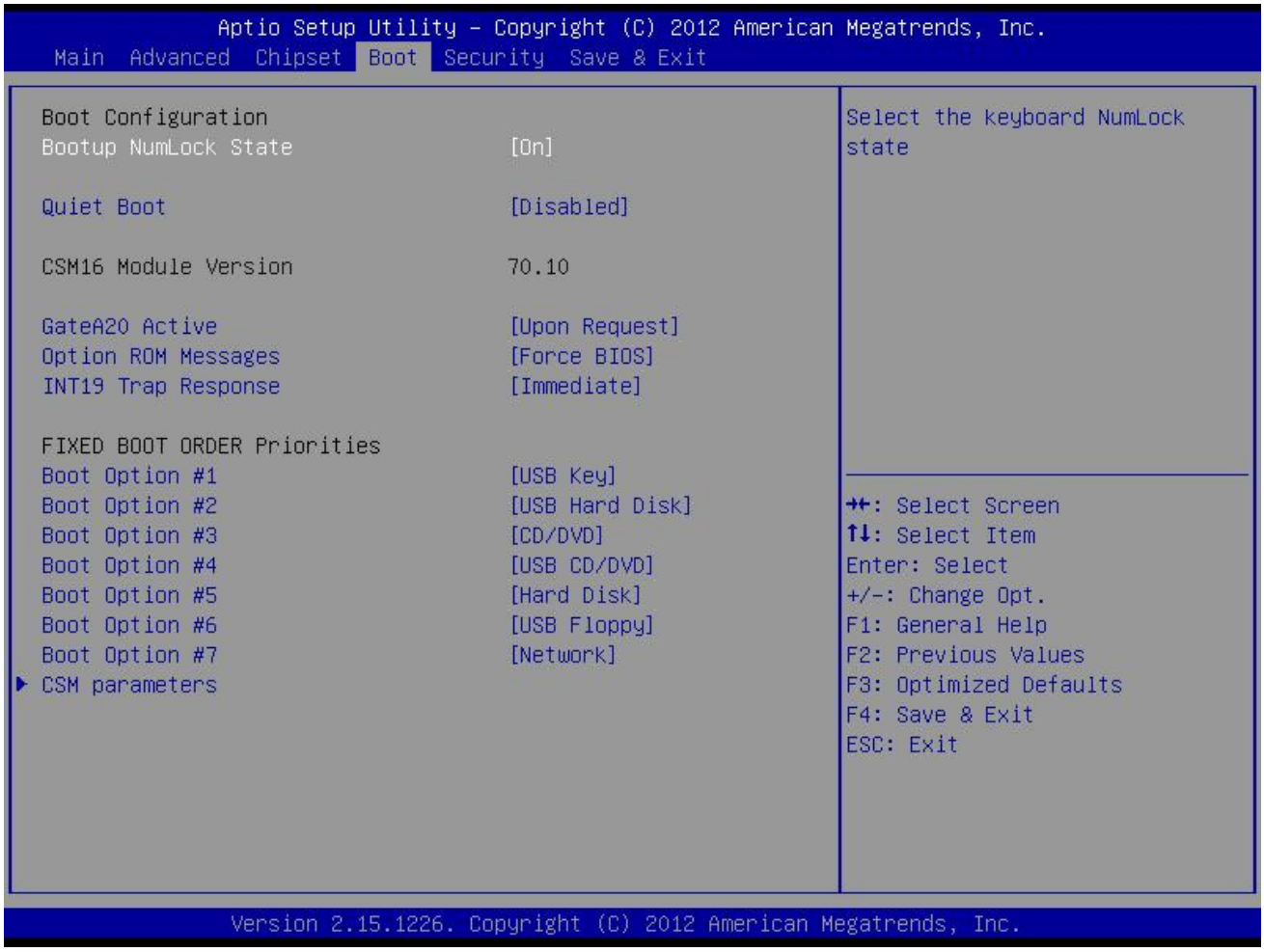
Default setting is <Auto>


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Chipset
Memory Configuration
Memory Clock [Auto]
Memory Hole Remapping [Enabled]
Bank Interleaving [Enabled]
Channel Interleaving [Enabled]
This Option Allows User to select different Memory Clock. Default value is 800Mhz.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

- 3.4 Boot Menu

Boot Configuration:

Description: This feature allows the user to specify which devices are boot devices and the order of priority from which the systems boots from during startup.


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Boot Configuration
Bootup NumLock State [On]
Quiet Boot [Disabled]
CSM16 Module Version 70.10
GateA20 Active [Upon Request]
Option ROM Messages [Force BIOS]
INT19 Trap Response [Immediate]
FIXED BOOT ORDER Priorities
Boot Option #1 [USB Key]
Boot Option #2 [USB Hard Disk]
Boot Option #3 [CD/DVD]
Boot Option #4 [USB CD/DVD]
Boot Option #5 [Hard Disk]
Boot Option #6 [USB Floppy]
Boot Option #7 [Network]
CSM parameters
Select the keyboard NumLock state
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

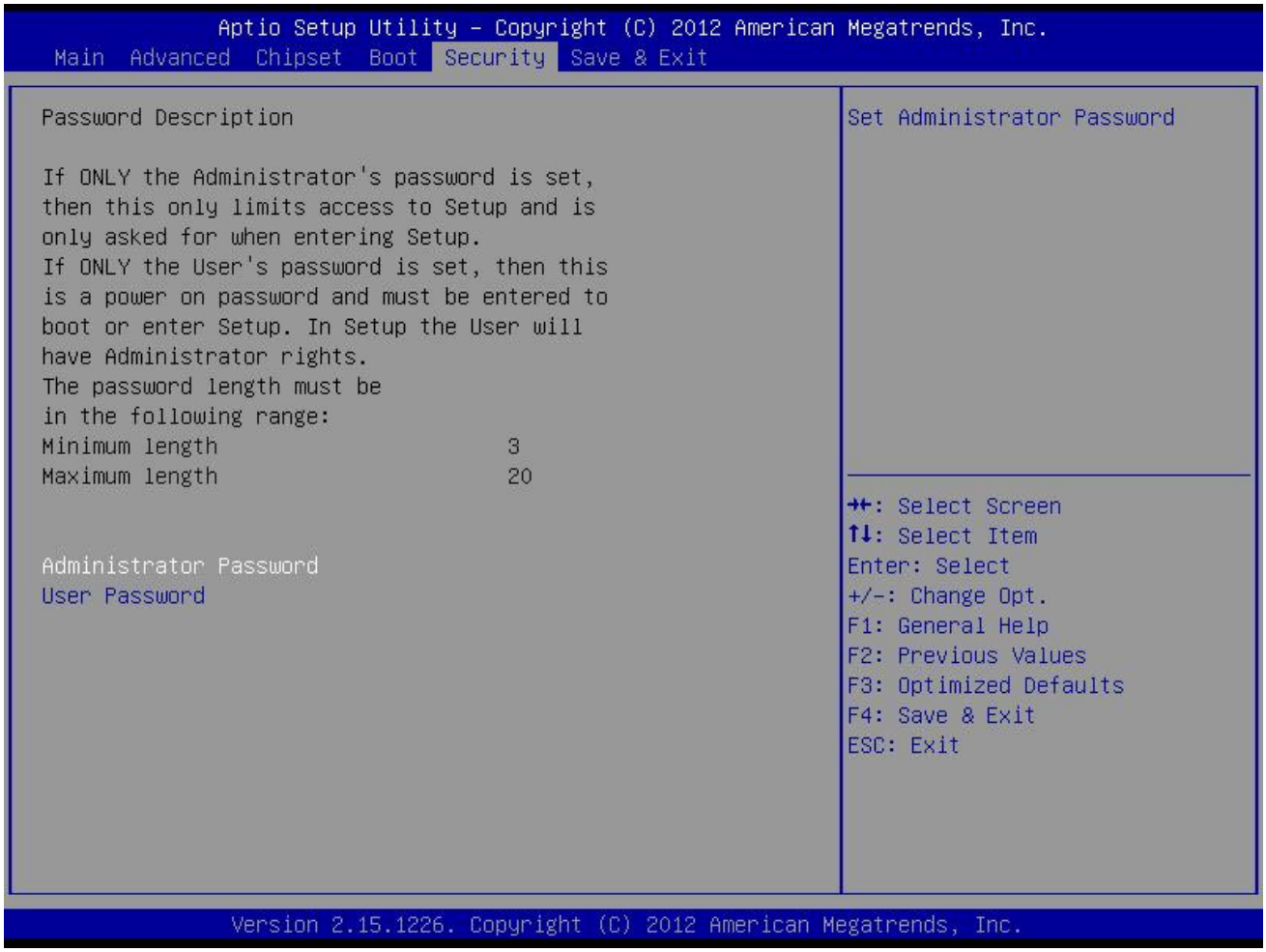
- 3.5 Security Menu

Password Description:

Description:

Administrator Password : Press Enter to create a new, or change an existing Administrator password.

User Password : Press Enter to create a new, or change an existing User password.


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Password Description
If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup.
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights.
The password length must be in the following range:
Minimum length 3
Maximum length 20
Administrator Password
User Password
Set Administrator Password
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

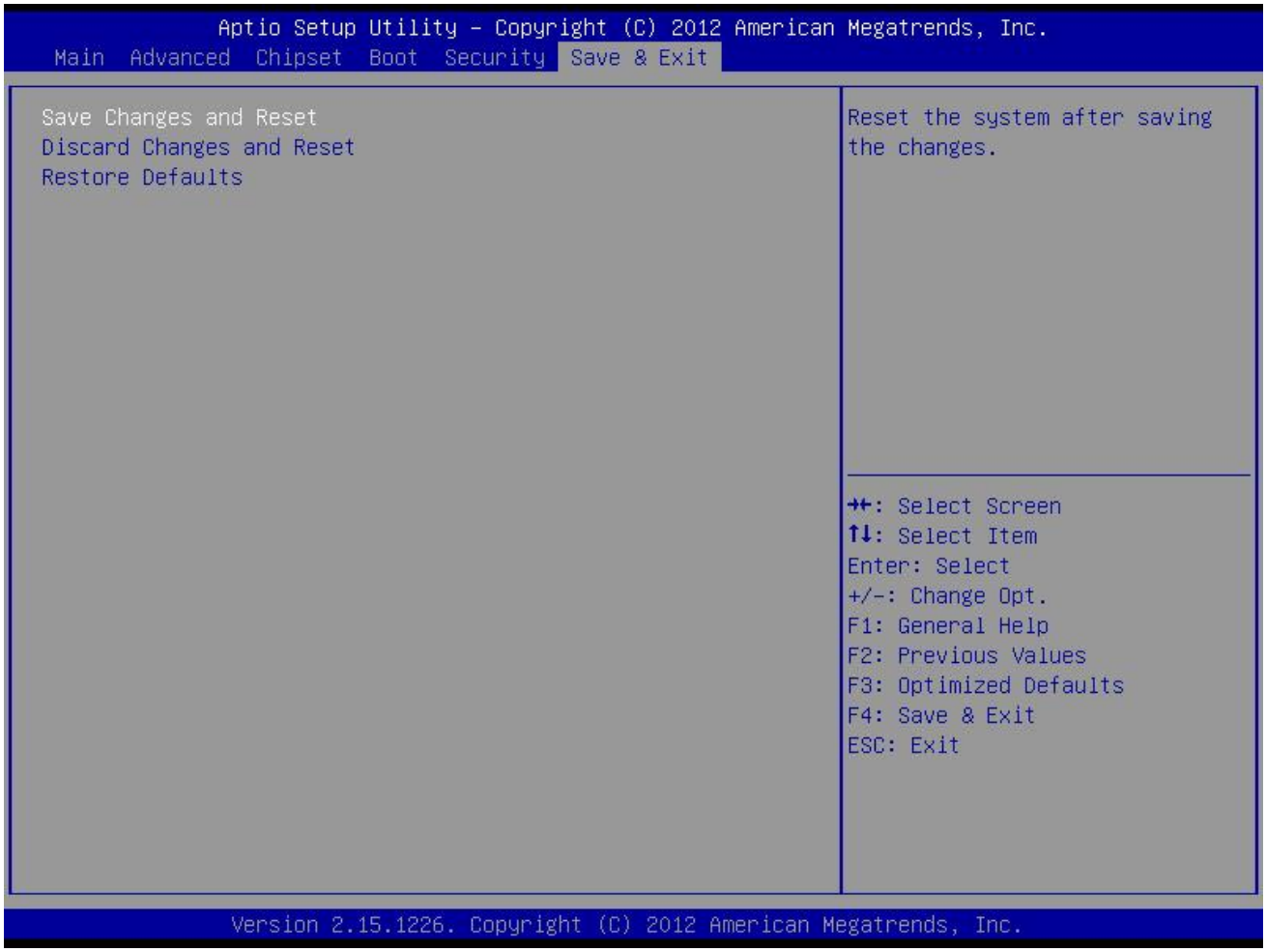
- 3.6 Save & Exit Menu

Description:

Save Change and Reset : When you have completed the system configuration changes, select this option to leave the BIOS Setup Utility and reboot the computer, so the new system configuration parameters can take effect. Select Save Changes and Exit from the Exit menu and press <Enter>

Discard Changes and Reset : Select this option to quit the BIOS Setup without making any permanent changes to the system configuration, and reboot the computer. Select Discard Changes and Exit from the Exit menu and press <Enter>.

Restored Defaults : To set this feature, select Restore Defaults from the Exit menu and press <Enter>. These are factory settings designed for maximum system stability, but not for maximum performance.


Aptio Setup Utility – Copyright (C) 2012 American Megatrends, Inc.
Main Advanced Chipset Boot Security Save & Exit
Save Changes and Reset
Discard Changes and Reset
Restore Defaults
Reset the system after saving the changes.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.15.1226. Copyright (C) 2012 American Megatrends, Inc.

4. GPIO and WatchDpg Timer sample code

- 4.1 GPIO Sample Program for DOS environment

```
//AEWIN    GPIO Program for MB-8390(DOS Version)
#include <stdio.h>
#include <string.h>
#include <dos.h>
#include <stdlib.h>
#include <inlines/pc.h>

#define index_port  0x4E
#define data_port    0x4f

void help();
void Enter_SIO();
void Exit_SIO();

int main(int argc, char *argv[])
{
      int data_rw8, val;

      if (argc!=2){
            help();
            return;
      }

      Enter_SIO();
      if(strcmp(argv[1], "-80h") == 0){
            val = 0x01;
            outportb(index_port, 0x89);
            data_rw8 = inportb(data_port)&(~val);
            data_rw8 |= val;
            outportb(data_port, data_rw8);
            printf("(Set GP80 to high)\n");
      }
      else if(strcmp(argv[1], "-80l") == 0){
```

```
        val = 0x01;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP80 to low)\n");
    }
    else if(strcmp(argv[1], "-81h") == 0){
        val = 0x02;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP81 to high)\n");
    }
    else if(strcmp(argv[1], "-81l") == 0){
        val = 0x02;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP81 to low)\n");
    }
    else if(strcmp(argv[1], "-82h") == 0){
        val = 0x04;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP82 to high)\n");
    }
    else if(strcmp(argv[1], "-82l") == 0){
        val = 0x04;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP82 to low)\n");
    }
    else if(strcmp(argv[1], "-83h") == 0){
```

```
        val = 0x08;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP83 to high)\n");
    }
    else if(strcmp(argv[1], "-83l") == 0){
        val = 0x08;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP83 to low)\n");
    }
    else if(strcmp(argv[1], "-84h") == 0){
        val = 0x10;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP84 to high)\n");
    }
    else if(strcmp(argv[1], "-84l") == 0){
        val = 0x10;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP84 to low)\n");
    }
    else if(strcmp(argv[1], "-85h") == 0){
        val = 0x20;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP85 to high)\n");
    }
```

```
else if(strcmp(argv[1], "-85l") == 0){
        val = 0x20;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP85 to low)\n");
}
else if(strcmp(argv[1], "-86h") == 0){
        val = 0x40;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP86 to high)\n");
}
else if(strcmp(argv[1], "-86l") == 0){
        val = 0x40;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP86 to low)\n");
}
else if(strcmp(argv[1], "-87h") == 0){
        val = 0x80;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP87 to high)\n");
}
else if(strcmp(argv[1], "-87l") == 0){
        val = 0x80;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&(~val);
        outportb(data_port, data_rw8);
        printf("(Set GP87 to low)\n");
}
```

```
else if(strcmp(argv[1], "-hhh") == 0){
        val = 0xFF;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port);
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP80~87 to high)\n");
}
else if(strcmp(argv[1], "-lll") == 0){
        val = 0x00;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port);
        data_rw8 &= val;
        outportb(data_port, data_rw8);
        printf("(Set GP80~87 to low)\n");
}
else if(strcmp(argv[1], "-lte") == 0){
        val = 0x0F;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&0x00;
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP80~83 to high, GP84~87 to low)\n");
}
else if(strcmp(argv[1], "-ltd") == 0){
        val = 0xF0;
        outportb(index_port, 0x89);
        data_rw8 = inportb(data_port)&0x00;
        data_rw8 |= val;
        outportb(data_port, data_rw8);
        printf("(Set GP80~83 to low, GP84~87 to high)\n");
}
else if(strcmp(argv[1], "-gpr") == 0){
        outportb(index_port, 0x8A);

        val = 0x01;
        data_rw8 = inportb(data_port)&(val);
```

```
if(data_rw8==val)printf("(GP80 is high)\n");
else printf("(GP80 is low)\n");

val = 0x02;
data_rw8 = inportb(data_port)&(val);
if(data_rw8==val)printf("(GP81 is high)\n");
else printf("(GP81 is low)\n");

val = 0x04;
data_rw8 = inportb(data_port)&(val);
if(data_rw8==val)printf("(GP82 is high)\n");
else printf("(GP82 is low)\n");

val = 0x08;
data_rw8 = inportb(data_port)&(val);
if(data_rw8==val)printf("(GP83 is high)\n");
else printf("(GP83 is low)\n");

val = 0x10;
data_rw8 = inportb(data_port)&(val);
if(data_rw8==val)printf("(GP84 is high)\n");
else printf("(GP84 is low)\n");

val = 0x20;
data_rw8 = inportb(data_port)&(val);
if(data_rw8==val)printf("(GP85 is high)\n");
else printf("(GP85 is low)\n");

val = 0x40;
data_rw8 = inportb(data_port)&(val);
if(data_rw8==val)printf("(GP86 is high)\n");
else printf("(GP86 is low)\n");

val = 0x80;
data_rw8 = inportb(data_port)&(val);
if(data_rw8==val)printf("(GP87 is high)\n");
else printf("(GP87 is low)\n");
```

```
	}
	else{
		help();
	}

	Exit_SIO();
	return;
}

void Enter_SIO()
{
	outportb(index_port, 0x87);
	delay(1);
	outportb(index_port, 0x87);
	outportb(index_port, 0x07);
	outportb(data_port,    0x06);
}

void Exit_SIO()
{
	outportb(index_port, 0xAA);
}

void help()
{
	printf("AEWIN GPIO test program\n");
	printf("=============================================\n");
	printf("gpio -hhh (Set GP80~87 to high)\n");
	printf("gpio -lll (Set GP80~87 to low )\n");
	printf("gpio -lte (Set GP80~83 to high, GP84~87 to low)\n");
	printf("gpio -ltd (Set GP80~83 to low, GP84~87 to high)\n");
	printf("gpio -gpr (Read GPIO status)\n");
	printf("gpio -xxh (Set xx to high)\n");
	printf("gpio -xxl (Set xx to low)\n");
	printf("       (xx=80~87)\n");
	printf("=============================================\n");
}
```

4.2 Watchdog timer Sample Program for DOS environment

```
//AEWIN Watch dog program for MB-8390(Dos Version)
#include <stdio.h>
#include <string.h>
#include <dos.h>
#include <stdlib.h>
#include <inlines/pc.h>

#define index_port  0x4E                    //Super IO Index port address
#define data_port    0x4F                   //Super IO Data port address

void Enter_sio_config();
void Exit_sio_config();
void help();

int main(int argc, char *argv[])
{
      int data_rw8, time;

            if (argc<2){
            help();
            return;
      }

            if(strcmp(argv[1], "-s") == 0){
                  //Show Watchdog Register Settings
            Enter_sio_config();
            outportb(index_port, 0xF5);
            data_rw8 = inportb(data_port)&0x08;
            if(data_rw8 == 0x00){
                  //second mode
                  outportb(index_port, 0xF6);
                  data_rw8 = inportb(data_port);
                  printf("Second mode: %d second\n", data_rw8);
            }
```

```
        else{
            //minute mode
            outportb(index_port, 0xF6);
            data_rw8 = inportb(data_port);
            printf("Minute mode: %d minute\n", data_rw8);
        }
        }
    else if(strcmp(argv[1], "-t") ==0 ){
        //Set Time-out Value
        if(argv[2] == NULL){
            help();
            return;
        }
        else{
            Enter_sio_config();
            outportb(index_port, 0xF6);
            outportb(data_port , 0x00);                    //Clear Status
            outportb(index_port, 0xF5);
            data_rw8 = 0x32;
            outportb(data_port, data_rw8);
                sscanf(argv[2], "%d", &time);
            outportb(index_port, 0xF6);
            outportb(data_port,    time);
            if(time==0){
                //Disable count
                outportb(index_port, 0xF5);
                data_rw8 = inportb(data_port)&0xCF;
                outportb(data_port , data_rw8);
            }
            else{
                outportb(index_port, 0xFA);
                outportb(data_port , 0x01);                //Enable reset function
            }
                printf("Watchdog Timer will count down for %d second(s)\n", time);
        }
    }
    else if(strcmp(argv[1], "-m") ==0 ){
```

```
        //Set Time-out Value
        if(argv[2] == NULL){
            help();
            return;
        }
        else{
            Enter_sio_config();
            outportb(index_port, 0xF6);
            outportb(data_port , 0x00);                    //Clear Status
            outportb(index_port, 0xF5);
            data_rw8 = 0x32;
            data_rw8 |= 0x08;
            outportb(data_port, data_rw8);
                sscanf(argv[2], "%d", &time);
            outportb(index_port, 0xF6);
            outportb(data_port,    time);
            if(time==0){
                //Disable count
                outportb(index_port, 0xF5);
                data_rw8 = inportb(data_port)&0xCF;
                outportb(data_port , data_rw8);
            }
            else{
                outportb(index_port, 0xFA);
                outportb(data_port , 0x01);                //Enable reset function
            }
                printf("Watchdog Timer will count down for %d minute(s)\n", time);
        }
    }
    Exit_sio_config();
    return;
}

void Enter_sio_config()                    //Enter W83627EHF Configuration
{
    outportb(index_port, 0x87);
    delay(1);                              //Delay some time
```

```
    outportb(index_port, 0x87);
    outportb(index_port, 0x07);          //Super IO Selct Bank Register Number
    outportb(data_port , 0x07);          //Select logical device 7
}

void Exit_sio_config()                   //Exit W83627EHF Configuration
{
    outportb(index_port, 0xAA);
}

void help()
{
    printf("AEWIN Watchdog Timer Program\n");
    printf("Usage: WDT -s        (Show Watchdog Register Settings)\n");
    printf("Usage: WDT -t xxx (Set Time-out Value)\n");
    printf("                xxx = 1 ~ 255 seconds\n");
    printf("                xxx = 0 : Time-out Disable \n");
    printf("Usage: WDT -m xxx (Set Time-out Value)\n");
    printf("                xxx = 1 ~ 255 minutes\n");
    printf("                xxx = 0 : Time-out Disable \n");
}
```

Device Resources

Resource	Share	Device Description	
	DMA 04	Exclusive	Direct memory access controller
	IRQ 00	Exclusive	System timer
	IRQ 03	Exclusive	Communications Port (COM2)
	IRQ 04	Exclusive	Communications Port (COM1)
	IRQ 05	Shared	Ethernet Controller
	IRQ 07	Exclusive	Communications Port (COM3)
	IRQ 08	Exclusive	System CMOS/real time clock
	IRQ 10	Shared	Universal Serial Bus (USB) Controller
	IRQ 100	Exclusive	Microsoft ACPI-Compliant System
	IRQ 101	Exclusive	Microsoft ACPI-Compliant System
	IRQ 102	Exclusive	Microsoft ACPI-Compliant System
	IRQ 103	Exclusive	Microsoft ACPI-Compliant System
	IRQ 104	Exclusive	Microsoft ACPI-Compliant System
	IRQ 105	Exclusive	Microsoft ACPI-Compliant System
	IRQ 106	Exclusive	Microsoft ACPI-Compliant System
	IRQ 107	Exclusive	Microsoft ACPI-Compliant System
	IRQ 108	Exclusive	Microsoft ACPI-Compliant System
	IRQ 109	Exclusive	Microsoft ACPI-Compliant System
	IRQ 11	Shared	Ethernet Controller
	IRQ 11	Shared	Universal Serial Bus (USB) Controller
	IRQ 110	Exclusive	Microsoft ACPI-Compliant System
	IRQ 111	Exclusive	Microsoft ACPI-Compliant System
	IRQ 112	Exclusive	Microsoft ACPI-Compliant System
	IRQ 113	Exclusive	Microsoft ACPI-Compliant System
	IRQ 114	Exclusive	Microsoft ACPI-Compliant System
	IRQ 115	Exclusive	Microsoft ACPI-Compliant System

IRQ 116	Exclusive	Microsoft ACPI-Compliant System
IRQ 117	Exclusive	Microsoft ACPI-Compliant System
IRQ 118	Exclusive	Microsoft ACPI-Compliant System
IRQ 119	Exclusive	Microsoft ACPI-Compliant System
IRQ 120	Exclusive	Microsoft ACPI-Compliant System
IRQ 121	Exclusive	Microsoft ACPI-Compliant System
IRQ 122	Exclusive	Microsoft ACPI-Compliant System
IRQ 123	Exclusive	Microsoft ACPI-Compliant System
IRQ 124	Exclusive	Microsoft ACPI-Compliant System
IRQ 125	Exclusive	Microsoft ACPI-Compliant System
IRQ 126	Exclusive	Microsoft ACPI-Compliant System
IRQ 127	Exclusive	Microsoft ACPI-Compliant System
IRQ 128	Exclusive	Microsoft ACPI-Compliant System
IRQ 129	Exclusive	Microsoft ACPI-Compliant System
IRQ 13	Exclusive	Numeric data processor
IRQ 130	Exclusive	Microsoft ACPI-Compliant System
IRQ 131	Exclusive	Microsoft ACPI-Compliant System
IRQ 132	Exclusive	Microsoft ACPI-Compliant System
IRQ 133	Exclusive	Microsoft ACPI-Compliant System
IRQ 134	Exclusive	Microsoft ACPI-Compliant System
IRQ 135	Exclusive	Microsoft ACPI-Compliant System
IRQ 136	Exclusive	Microsoft ACPI-Compliant System
IRQ 137	Exclusive	Microsoft ACPI-Compliant System
IRQ 138	Exclusive	Microsoft ACPI-Compliant System
IRQ 139	Exclusive	Microsoft ACPI-Compliant System
IRQ 14	Exclusive	ATA Channel 0
IRQ 140	Exclusive	Microsoft ACPI-Compliant System
IRQ 141	Exclusive	Microsoft ACPI-Compliant System
IRQ 142	Exclusive	Microsoft ACPI-Compliant System
IRQ 143	Exclusive	Microsoft ACPI-Compliant System
IRQ 144	Exclusive	Microsoft ACPI-Compliant System
IRQ 145	Exclusive	Microsoft ACPI-Compliant System

IRQ 146	Exclusive	Microsoft ACPI-Compliant System
IRQ 147	Exclusive	Microsoft ACPI-Compliant System
IRQ 148	Exclusive	Microsoft ACPI-Compliant System
IRQ 149	Exclusive	Microsoft ACPI-Compliant System
IRQ 15	Exclusive	ATA Channel 1
IRQ 150	Exclusive	Microsoft ACPI-Compliant System
IRQ 151	Exclusive	Microsoft ACPI-Compliant System
IRQ 152	Exclusive	Microsoft ACPI-Compliant System
IRQ 153	Exclusive	Microsoft ACPI-Compliant System
IRQ 154	Exclusive	Microsoft ACPI-Compliant System
IRQ 155	Exclusive	Microsoft ACPI-Compliant System
IRQ 156	Exclusive	Microsoft ACPI-Compliant System
IRQ 157	Exclusive	Microsoft ACPI-Compliant System
IRQ 158	Exclusive	Microsoft ACPI-Compliant System
IRQ 159	Exclusive	Microsoft ACPI-Compliant System
IRQ 16	Shared	High Definition Audio Controller
IRQ 16	Shared	PCI standard PCI-to-PCI bridge
IRQ 160	Exclusive	Microsoft ACPI-Compliant System
IRQ 161	Exclusive	Microsoft ACPI-Compliant System
IRQ 162	Exclusive	Microsoft ACPI-Compliant System
IRQ 163	Exclusive	Microsoft ACPI-Compliant System
IRQ 164	Exclusive	Microsoft ACPI-Compliant System
IRQ 165	Exclusive	Microsoft ACPI-Compliant System
IRQ 166	Exclusive	Microsoft ACPI-Compliant System
IRQ 167	Exclusive	Microsoft ACPI-Compliant System
IRQ 168	Exclusive	Microsoft ACPI-Compliant System
IRQ 169	Exclusive	Microsoft ACPI-Compliant System
IRQ 17	Shared	Standard Enhanced PCI to USB Host Controller
IRQ 17	Shared	Standard Enhanced PCI to USB Host Controller
IRQ 17	Shared	PCI standard PCI-to-PCI bridge
IRQ 170	Exclusive	Microsoft ACPI-Compliant System
IRQ 171	Exclusive	Microsoft ACPI-Compliant System

IRQ 172	Exclusive	Microsoft ACPI-Compliant System
IRQ 173	Exclusive	Microsoft ACPI-Compliant System
IRQ 174	Exclusive	Microsoft ACPI-Compliant System
IRQ 175	Exclusive	Microsoft ACPI-Compliant System
IRQ 176	Exclusive	Microsoft ACPI-Compliant System
IRQ 177	Exclusive	Microsoft ACPI-Compliant System
IRQ 178	Exclusive	Microsoft ACPI-Compliant System
IRQ 179	Exclusive	Microsoft ACPI-Compliant System
IRQ 18	Shared	Standard OpenHCD USB Host Controller
IRQ 18	Shared	Standard OpenHCD USB Host Controller
IRQ 18	Shared	Standard OpenHCD USB Host Controller
IRQ 18	Shared	High Definition Audio Controller
IRQ 180	Exclusive	Microsoft ACPI-Compliant System
IRQ 181	Exclusive	Microsoft ACPI-Compliant System
IRQ 182	Exclusive	Microsoft ACPI-Compliant System
IRQ 183	Exclusive	Microsoft ACPI-Compliant System
IRQ 184	Exclusive	Microsoft ACPI-Compliant System
IRQ 185	Exclusive	Microsoft ACPI-Compliant System
IRQ 186	Exclusive	Microsoft ACPI-Compliant System
IRQ 187	Exclusive	Microsoft ACPI-Compliant System
IRQ 188	Exclusive	Microsoft ACPI-Compliant System
IRQ 189	Exclusive	Microsoft ACPI-Compliant System
IRQ 19	Shared	PCI standard PCI-to-PCI bridge
IRQ 19	Shared	Standard AHCI 1.0 Serial ATA Controller
IRQ 190	Exclusive	Microsoft ACPI-Compliant System
IRQ 81	Exclusive	Microsoft ACPI-Compliant System
IRQ 82	Exclusive	Microsoft ACPI-Compliant System
IRQ 83	Exclusive	Microsoft ACPI-Compliant System
IRQ 84	Exclusive	Microsoft ACPI-Compliant System
IRQ 85	Exclusive	Microsoft ACPI-Compliant System
IRQ 86	Exclusive	Microsoft ACPI-Compliant System
IRQ 87	Exclusive	Microsoft ACPI-Compliant System

IRQ 88	Exclusive	Microsoft ACPI-Compliant System
IRQ 89	Exclusive	Microsoft ACPI-Compliant System
IRQ 90	Exclusive	Microsoft ACPI-Compliant System
IRQ 91	Exclusive	Microsoft ACPI-Compliant System
IRQ 92	Exclusive	Microsoft ACPI-Compliant System
IRQ 93	Exclusive	Microsoft ACPI-Compliant System
IRQ 94	Exclusive	Microsoft ACPI-Compliant System
IRQ 95	Exclusive	Microsoft ACPI-Compliant System
IRQ 96	Exclusive	Microsoft ACPI-Compliant System
IRQ 97	Exclusive	Microsoft ACPI-Compliant System
IRQ 98	Exclusive	Microsoft ACPI-Compliant System
IRQ 99	Exclusive	Microsoft ACPI-Compliant System
Memory 000A0000-000BFFFF	Shared	Standard VGA Graphics Adapter
Memory 000A0000-000BFFFF	Shared	PCI bus
Memory 000C0000-000DFFFF	Shared	PCI bus
Memory 60000000-7FFFFFFF	Exclusive	Motherboard resources
Memory 80000000-FFFFFFFF	Shared	PCI bus
Memory D0000000-DFFFFFFF	Exclusive	Standard VGA Graphics Adapter
Memory E0000000-EFFFFFFF	Exclusive	System board
Memory FE900000-FE91FFFF	Exclusive	Ethernet Controller
Memory FE900000-FE9FFFFF	Exclusive	PCI standard PCI-to-PCI bridge
Memory FE920000-FE923FFF	Exclusive	Ethernet Controller
Memory FEA00000-FEA1FFFF	Exclusive	Ethernet Controller
Memory FEA00000-FEAFFFFF	Exclusive	PCI standard PCI-to-PCI bridge
Memory FEA20000-FEA23FFF	Exclusive	Ethernet Controller
Memory FEB00000-FEB3FFFF	Exclusive	Standard VGA Graphics Adapter
Memory FEB40000-FEB43FFF	Exclusive	High Definition Audio Controller
Memory FEB44000-FEB47FFF	Exclusive	High Definition Audio Controller
Memory FEB48000-FEB49FFF	Exclusive	Universal Serial Bus (USB) Controller
Memory FEB4A000-FEB4BFFF	Exclusive	Universal Serial Bus (USB) Controller
Memory FEB4C000-FEB4CFFF	Exclusive	Standard OpenHCD USB Host Controller
Memory	Exclusive	Standard Enhanced PCI to USB Host Controller

FEB4D000-FEB4D0FF		
Memory FEB4E000-FEB4EFFF	Exclusive	Standard OpenHCD USB Host Controller
Memory FEB4F000-FEB4F0FF	Exclusive	Standard Enhanced PCI to USB Host Controller
Memory FEB50000-FEB50FFF	Exclusive	Standard OpenHCD USB Host Controller
Memory FEB51000-FEB517FF	Exclusive	Standard AHCI 1.0 Serial ATA Controller
Memory FEC00000-FEC00FFF	Exclusive	Motherboard resources
Memory FEC10000-FEC10FFF	Exclusive	Motherboard resources
Memory FED00000-FED003FF	Exclusive	High precision event timer
Memory FED00000-FED00FFF	Exclusive	Motherboard resources
Memory FED40000-FED44FFF	Exclusive	Unknown
Memory FED61000-FED70FFF	Exclusive	Motherboard resources
Memory FED80000-FED8FFFF	Exclusive	Motherboard resources
Memory FEE00000-FEE00FFF	Exclusive	Motherboard resources
Memory FF000000-FFFFFFFF	Exclusive	Motherboard resources